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received and stored through a communication channel or an appropriate storage medium as required, while at the same time receiving a specified digital signal by the connection through a connector with the memory card having playback function (player). Further, the memory capacity of the terminal device is equal to or more than that of the memory on the memory card with playback function, and the terminal device is used with a hard disk memory unit having a comparatively large memory capacity as a backup memory. At the same time, the digital signal frequently received and delivered with the memory card having the playback function or the digital signal updated with the lapse of time is stored in a buffer memory configured of a semiconductor memory accessible at high speed, thereby making possible efficient receiving and delivery of information. Furthermore, the storage area of a memory in the memory card with playback function is controlled. In addition, the abovementioned terminal device realizes a digital information system having the function of audition with a part of designated digital signals reproduced and outputted over a predetermined length of time, and having an ultrasmall, ultrathin memory card with playback function as the result of slow/fast playback by voice interval control and neglection of quantizing noises.

The player receives a digital signal in the form of electrical signal, and independently play backs, so that the value of the digital signal received can be exhibited in direct form. As a consequence of the usability of a digital signal in direct form, a system for processing, production and sale thereof is configured easily. At the same time, the simple player construction in the form of an ultrasmall, ultrathin card, offers the handling ease for every user. By enlarging or extending the voice interval of the digital audio signal substantially, the slow or fast playback is made possible without deteriorating the audio quality.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the essential parts of a digital information system according to an embodiment of the present invention;
Fig. 2 is a block diagram showing an input section of the terminal device of Fig. 1;
Fig. 3 is a block diagram showing a memory section of the terminal device of Fig. 1;
Fig. 4 is a block diagram showing an output section of the terminal device of Fig. 1;
Fig. 5 is a block diagram showing the essential parts of a data input section of a player;
Fig. 6 is a block diagram showing the essential parts of a data output section of the terminal device of Fig. 1;
Fig. 7 is a block diagram showing an embodiment of the player used with a digital information system according to the present invention;
Fig. 8 is a plan view showing an embodiment of a package board configuring the player;
Fig. 9 is a side view showing an embodiment of a package board accommodated in a case;
Fig. 10 is a plan view showing another embodiment of the player;
Fig. 11 is a block diagram showing an embodiment of the player body and the memory section of Fig. 10;
Fig. 12 is a block diagram showing an embodiment of a power supply system of the player;
Fig. 13 is a diagram showing the configuration of an embodiment of the digital signal transferred from a terminal device to the player;
Fig. 14 is a block diagram showing an embodiment of the player corresponding to the digital signal with the ID signal of Fig. 13 inserted therein;
Fig. 15 is a circuit diagram showing an embodiment of a quantizing noise remover according to the present invention;
Fig. 16 is a diagram showing waveforms for explaining an example of the operation of the quantizing noise remover of Fig. 15;
Fig. 17 is a circuit diagram showing an embodiment of a security circuit used in a digital signal selling system according to the present invention;
Fig. 18 is a circuit diagram showing another embodiment of the security circuit used in a digital signal selling system according to the present invention;
Fig. 19 is a circuit diagram showing still another embodiment of the security circuit used with a digital signal selling system according to the present invention;
Fig. 20 is a circuit diagram showing a further embodiment of the security circuit used in a digital signal selling system according to the present invention;
Fig. 21 is a circuit diagram showing a still further embodiment of the security circuit used in a digital signal selling system according to the present invention;
Fig. 22 is a specific circuit diagram showing an embodiment of a bit exchanger used in the security circuit of Fig. 21;
Fig. 23 is a circuit diagram showing an embodiment of the security circuit suitable for copy prevention used in a digital signal selling system according to the present invention;
Fig. 24 is a circuit diagram showing another embodiment of the security circuit suitable for copy prevention used in a digital signal selling system according to the present invention;
Fig. 25 is a circuit diagram showing still another embodiment of the security system suitable for copy prevention used in a digital signal selling system according to the present invention;

Fig. 64 is a full view of type II of memory card according to the JEIDA standard;
Fig. 65 is a table showing the pin arrangement of a memory card according to the JEIDA standard;
Fig. 66 is a table showing signal characteristics of a memory card according to the JEIDA standard;
Fig. 67 is a diagram specifically showing the appearance of an embodiment of a digital signal receiving/delivery system according to the present invention;
Fig. 68 is a diagram specifically showing the appearance of another embodiment of a digital information system according to the present invention; and
Fig. 69 is a diagram specifically showing the appearance of still another embodiment of a digital signal receiving/delivery system according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A block diagram of essential parts of a digital signal transmitting receiving system according to an embodiment of the present invention is shown in Fig. 1. This embodiment is intended for a system to commercialize and sell information of a digital signal. In other words, the sale of the information is made available as one of forms of transmitting receiving of a digital signal.

In Fig. 1 is shown a block diagram of a terminal device of a digital signal selling system. This terminal device 100 is equivalent to a vending machine for cigarettes or soft drinks such as juice and functions as an information server. The terminal equipment 100, is connected to an original supplier of a digital signal through a broad band integrated services digital network (B-ISDN) to receive the digital signal as a commodity without specific limitation. As a result of employment of this system, the digital signal is transferred only to a specified terminal device 100 through a communication network in a manner similar to such commodities as cigarettes and juice. In this case, the digital signal as a commodity can be transferred at high speed and in a great amount, free of any traffic jam or air pollution unlike in the case of general commodities. The terminal device 100 is installed in front of a store like a station booth, a cigar stand or a book shop.

The terminal device 100 is roughly comprised of an input section 102, a memory section 103 and an output section 104. Each circuit section, which is connected to a VME bus 105, is adapted to receive digital and various control signals. This terminal device 100, which is connected to a memory card 101 with a reproducing function (hereinafter called "the player") shown by dotted line in Fig. 1, is used to directly receive a specific signal as a commodity.

Fig. 2 is a block diagram showing an input section 102 of the terminal device 100. The input section 102 of the terminal device 100 has a VME interface 201 for the broad band integrated services digital network (B-ISDN) and an analog input interface (right and left analog inputs) for receiving an input signal in an analog form. The analog input interfaces are provided with low-pass filters 202a, 202b, associated with the right input Rin and the left input Lin, for eliminating extraneous frequency band components contained in the analog input signals Rin and Lin in advance, respectively. These input signals Rin and Lin are alternately selected through a multiplexer 203 with respect to time, introduced to a sample-and-hold circuit 204 and converted into a digital signal by an analog-to-digital converter 205. At this time, the analog-to-digital converter 205 outputs two-channel (stereo) time-shared digital signals of right and left channels in time series, which signals are introduced to the VME interface of the input section 207. Such analog input interfaces are used for digitalizing and storing music programs, regular news, stock market information, various commodity market situations or the like sent by broadcasting in a memory.

A monaural signal is inputted as the above-mentioned right or left input signal. The function may be added to broaden band widths of the low-pass filters 202a, 202b for input signals having a broad band widths such as music, and to narrow the band widths of the low-pass filters 202a, 202b for input signals having narrow band widths such as news. Reference numeral 206 designates an input section controller, and numeral 201 a network interface corresponding to the B-ISDN.

Each analog input interface may be adapted to receive a message from an automatic answering telephone set by being connected to a telephone line. In such a case, the function of a telephone set may be added to the terminal device 100 connected with the automatic answering telephone set to receive a recorded message therefrom. When the analog input interface is used in this way, the message transfer time is undesirably lengthened. If a subscriber to a digital line system uses a digital automatic answering telephone set to store messages in a digital form, the messages recorded can be received in a very short time, and by doing so, the user can confirm the messages, at the desired time while being in transportation means or under the like situation.

Fig. 3 is a block diagram showing a structure of an embodiment of the memory section in the terminal device 100. This memory section includes an external memory like a hard disk memory 301, a RAM (random access memory) 308 as a buffer memory, a ROM (read only memory) 307 for storing various programs, and a microprocessor 306 for processing information or performing control operations in accordance with these programs. The programs include the

cuit of the player 101 in unit of player. Specifically, the received commodity directly exhibits the value thereof as a commodity. These two features make the present invention conspicuously different from the conventional commodity transactions. Further, according to a system in which the player 101 is connected to the terminal device 100 and in which a digital signal is transmitted and received as a commodity as described above, only the required information can be specified and sold when required.

In Fig. 4, numeral 407 designates a power supply, which, though not specifically limited, supplies power from the terminal device 100 to the player 101 for the purpose of transmitting a high-speed digital signal, i.e., writing operation. Also, in the case where a rechargeable secondary battery is used as a power supply of the player 101 in place of the primary battery, as described later, or in the case where primary and secondary batteries are built in, a digital signal is transferred when the player 101 is connected to the terminal device 100. At the same time, the secondary battery is charged rapidly by the power supply 407. Signals transferred between the output section and the player 101 are an operating voltage V, a digital signal D, an address signal A, a control signal C or a status signal S, etc.

Also, in the cassette tape recorders commercially available at the present time, the time of information storage is equal to that of reproduction thereof in principle. This provides a great problem to the user in an information vending system proposed by the present invention. In a digital signal transmitting, receiving system, if the convenience of the user is taken into consideration, it is desirable to increase the speed of transfer of a digital signal between the terminal device 100 and the player 101 as far as possible. This function can be realized when a memory, a memory controller and data transfer means which can operate at least more rapidly than the signal to be reproduced, are provided in the buffer memory 403 of the terminal device output section 104 and the memory circuit 701 of the player 101 in Fig. 4.

This embodiment will be described with reference to Figs. 5 and 6. First, a block configuration relating to the high-speed transfer on the player 101 side is shown in Fig. 5. The player 101 is added therein with photo-sensor 502, an I-V amplifier 503, a serial-to-parallel converter 504, a PLL oscillator 505, a clock divider 506, a multiplexer 507 and a mode switch 508. In light mode (set when the mode switch 508 is switched to "light" side), the B inputs of the multiplexer 507 are selected to provide Y outputs, and therefore external write data supplied as a light pulse train (two start bits indicating "1" and "0" states are added to the head of the unit write data train) is written into the memory circuit 701. Specifically, a photo-modulated pulse train signal is converted into a current signal by the photo-sensor 501, and the waveform of the signal is shaped as a voltage signal by the I-V amplifier 503. This signal, after being inputted to the PLL oscillator 505 for extracting the clock components from the pulse train signal thus shaped, is also applied to the serial signal input terminal D of the serial-to-parallel converter 504 at the same time. A signal representing the clock components extracted by the PLL oscillator 505 (8 MHz in frequency according to the present invention) acts as a shift clock signal of the serial-to-parallel converter 504 and a count clock signal of the 1/n (n represents (the number of quantized bits) ÷2, or 10 according to the present invention) clock divider 506. An output signal (800 kHz according to this embodiment) of the clock divider 506 is a write strobe signal for the memory circuit 701.

In electricity mode (set when the mode switch is switched to "electricity" side), by contrast, the A inputs of the multiplexer 507 are selected to make up Y outputs, so that 8-bit parallel data is written into the memory circuit 701 from the input buffer 501 through the multiplexer 507.

Fig. 6 shows a block configuration of a data transmitting section of the terminal device 100. The 8-bit parallel data is outputted from the output buffer 601 as data of the buffer memory 403, and the data of the buffer memory 403 is converted into a serial signal by the parallel-to-serial converter 602 to generate a signal representing photo-modulated pulse train, and two start bits indicating the "1" and "0" states are added to the head of the pulse train by a start bit adding circuit 603. Further, a laser diode 605 is energized by the V-I amplifier 604, thereby to output the pulse train signal as a photo pulse train signal.

According to this embodiment, information such as an audio signal can be transferred by photo coupling at a high speed in wireless fashion. For example, the embodiment under consideration thus makes it possible to transfer the audio information of about six minutes (8 bits in resolution, 22.05 kHz in sampling frequency, and monaural) only for ten seconds. Also, in the case where the frequency of the clock signal is set to 800 kHz for reduction of power consumption upon the high-speed transfer, a satisfactory result is obtained although somewhat longer time is required.

The basic concept of the present embodiment lies in that the contents of a digital memory can be directly transferred, taking account for the fact that the operating speed of the digital memory such as a semiconductor memory is faster than transfer speed of an analog signal. Many applications of operation are of course possible within the framework of this concept. Apart from the photo-coupling system, for example, exactly the same result is obtained by connecting directly a data transfer source to a destination by connector, or as an alternative, the effect of application of electric wave or magnetism may be used. Further, in a system for transferring 8-bit parallel data, although the transmitting or receiving circuits simpli-

807 can be opened at the time of repair as described above, the electronic parts such as IC and LSI can be easily replaced.

Fig. 10 is a plan view showing another embodiment of the player 101.

In this embodiment, the body of the player 101 and the memory section 1001 are detachable. Specifically, the body of the player 101 includes, as in the case mentioned above, a control board 807 having thereon such ICs as a large-scale integrated circuit 709 for control operation, a digital-to-analog converter 707 and an amplifier 708, a battery case and a memory card connector 804 based on the JEIDA standard. As shown by dotted line in the drawing, there is provided an internal space for insertion of the memory section 1001 (memory card) in the form of thin card and a memory section connector 1103 shown in Fig. 11. The memory section 1001 has a pseudo-static RAM and a backup battery housed in a card-like thin plastic case, for example, as mentioned above. By making the memory Section 1001 detachable in this way, a plurality of types of memory card are made available. A variety of RAMs including the static RAM and dynamic RAM or the same type of RAM having a plurality of different storage capacities may be prepared. Also, in addition to these RAMs, the ROM card may be used. Not only the mask-type ROM but also EEPROM may be used for receiving digital signals. In the case where the EEPROM is used, the receiving of a digital signal, that is to say, the write operation thereof takes a little longer time than when the RAM is used. Nevertheless, the use of the backup battery is eliminated, thereby simplifying the production and handling of the memory card.

Further, the compatibility with the existing IC memory card is secured by adapting to the outline of the player 101 and the JEIDA standard employed for the general-purpose IC memory card including the physical specifications of the connector, etc., and such electrical specifications as the signal characteristics and timings and the card attribute information (The guide line Ver 4.0 is presently standardized). Although the outside dimensions, connector, pin arrangement, battery voltage, etc. are standardized according to the JEIDA standard, the outside dimensions, signal pin arrangement and signal characteristics are referred to specifically in this patent application. Fig. 63 shows an outline of the type I card according to the JEIDA standard. The outside dimensions of this card are

85.6 mm x 54.0 mm x 3.3 mm

Fig. 64 shows an outline of the type II card according to the JEIDA standard. The outside dimensions of this card are

85.6 mm x 54.0 mm x 5.5 mm

(3.3 mm for the connector section). Fig. 65 shows a signal pin arrangement, in which the number of pins is 68 for the guide line Ver 4.0. A signal characteristic is shown in Fig. 66.

Fig. 11 is a block diagram showing an embodiment of the body of the player 101 and the memory section 1001.

A memory card connector 804 based on the JEIDA standard to be connected with the terminal device 100 as described above is arranged on the outside of the body of the player 101. The player 101 has a memory section connector 1103 built therein. The card-like memory section 1001 is detachable through these memory section connectors 102, 1103.

The data inputted from the memory card connector 804 corresponding to the terminal device 100 is supplied to a data input terminal Di of the memory section 1001 through the memory section connectors 1002, 1103. The address inputted from the memory card connector corresponding to the terminal device 100 is supplied to an input A of the multiplexer 1105. The other input B of the multiplexer 1105 is supplied with a playback address as a memory address for playback generated by the address counter 1106 at the inside of the player 101. The address for receiving of a digital signal or the playback address is selectively supplied to the address terminal A of the memory section 1001 through the multiplexer 1105. The control signal inputted from the memory card connector 804 corresponding to the terminal device 100 is supplied to the input A of the multiplexer 1104. The other input B of the multiplexer 1104 is supplied with a playback control signal generated by the controller 1101 of the body of the player 101. The control signal for receiving of the digital and the playback control signal is selectively supplied to the control terminal C of the memory section 1001 through the multiplexer 1104.

In the manner mentioned above, the multiplexers 1105, 1104 are provided for switching the addresses or the control signals so as to selectively perform one of the receiving of the digital signal in accessing the memory section 1001 from the terminal device 100 side and the playback of the digital signal in accessing through the address counter 1106 or controller 1101 at the inside of the player 101. In this playback operation, the digital signal outputted from the output terminal Do upon the read operation of the memory section 1001 is outputted as an audio signal through the memory section connectors 1002, 1003 and a playback circuit including the low-pass filter 706, the digital-to-analog converter 707 and the amplifier 708 at the inside of the player 101.

The controller 1101 at the inside of the player 101 is adapted to control the digital-to-analog converter 707 and the low-pass filter 706 mentioned above in accordance with the ID code or the like of the reproduced digital signal.

The power supplied from the terminal device 100, on the other hand, is used also as an operating voltage for high-speed writing of the digital signal into the memory section 1001 connected through the mem-

cuit 701 is taken into a register 1401 by being regarded as the ID code 1308. Of all the ID codes 1308 taken into the register 1401, the codes 1300 (DO), 1301 (D1) are inputted to the multiplexer 1404, so that a clock pulse corresponding to the sampling rate among four clock pulses formed by the clock generator 1403 is selected and transmitted to the controller 704. The clock generator 1403 forms four clock pulses corresponding to the sampling rates in response to a reference frequency signal formed by the oscillator 1402.

Also, the code 1302 (D2) is inputted to a bit length converter 1405. The bit length converter 1405 has the function of parallel-to-serial conversion and inputs to a low-pass filter 706 a digital signal outputted from the memory circuit 701 in maximum units of two bytes in accordance with the bit length designated by 1302 (D2). The low-pass filter 706, including a digital filter, receives a clock pulse corresponding to the sampling rate from the controller 704 and cuts an extraneous frequency band of the input digital signal. Also, the digital-to-analog converter 707 converts an input digital signal into an analog signal in response to a clock pulse corresponding to the sampling rate from the controller 704. The amplifier 708 is for amplifying the analog signal thus converted thereby to form a drive signal such as for headphone. Although not shown in the drawing, the output section of the digital-to-analog converter 707 has a low-pass filter including a resistor and a capacitor.

The ID code 1308, though not specifically limited, includes eight bits of 1300 to 1307 (D0 to D7), of which 1300, 1301 (D0 and D1) are used to designate four sampling frequencies. The frequency 5.5125 kHz is designated when 1300 and 1301 are 00, 11.025 kHz when 1300 and 1301 are 01, 22.05 kHz when 1300 and 1301 are 10, and 44.1 kHz when 1300 and 1301 are 11. 1302 is used for designating the resolution. Eight bits are designated when it is 0, and 16 bits when it is 1. On the other hand, 1303 (D3) is used for mode designation, setting "monaural" when it is 0 and "stereo" when it is 1. The remaining four bits 1304 to 1307 (D4 to D7) are reserved for extension.

The relationship between the memory capacity (total number M of bits) of the memory circuit 701, the bit length N as a resolution, the sampling rate fs, the mode S (assuming that stereo S = 2 for stereo mode, and S = 1 for monaural mode) and the recording/playback time t is expressed by equation (1) below.

$$t = M/(N \times fs \times S) \quad (1)$$

As the sampling rate mentioned above, though not specifically limited, 44.1 kHz is used for playback of an ultra HiFi music program equivalent to the compact disk player, 22.05 kHz for playback of a HiFi music program, 11.024 kHz for playback of an information program such as news, and 5.5125 kHz for playback of an automatic answering telephone set, or the like. As described above, if the sampling frequency is set in units of double, the player 101 may form one reference frequency corresponding to say, 44.1 kHz, and by dividing it in units of 1/2, can easily form the sampling frequency. As a consequence, the recording/playback time is lengthened in reverse proportion to the four sampling frequencies fs described above. In other words, if a predetermined recording/playback time is to be obtained, the storage capacity is increased in proportion to the sampling rate fs.

In the case where the bit length is increased from 8 to 16 bits, the recording/playback time is doubled as will be seen from equation (1) above. With the increase in bit length, a double storage capacity is required of the memory circuit 701 to meet the increase. If the bit length is reduced to 8 bits, by contrast, the recording/playback time is increased to double for the same storage capacity. In stereo mode, specifically, a double data is required as compared with when the system is in monaural mode. More specifically, in stereo mode when right and left signals are outputted alternately from the memory circuit 701, the required storage capacity doubles from that required in monaural mode.

According to this embodiment, the three playback conditions including sampling rate, bit length and mode are set for a digital signal source as described above, and are combined as desired to permit playback, whereby the limited storage capacity of the memory can be utilized to the maximum efficiency. The playback conditions which can be combined in a great variety can be automatically set in the player 101 by the use of the ID code 1308, and therefore any user can easily reproduce the information received without any operating inconvenience.

The type or frequency of the sampling rate can be set as desired. In such a case, an arrangement should be made to generate a clock pulse in accordance with each sampling rate. Also, the ID code 1308 may have added thereto a bit that can be designated by the operation of a terminal device. By setting the slow or fast playback mode automatically by means of the remaining bits as explained later, for example, a playback mode such as reproduction by program or continuous reproduction for the whole program may be designated automatically.

Fig. 15 is a circuit diagram showing an embodiment of a quantizing noise remover.

When an analog signal is quantized, a quantizing noise (error component) is always generated. This quantizing noise is offensive to the ear especially during a voice interval. According to the present embodiment, a quantizing noise remover as described below is inserted in the input of the digital-to-analog converter 707.

The digital signal read out of the memory circuit 701 is inputted to the digital-to-analog converter 707 and is converted into an analog signal Vout. The quantizing noise remover according to the present

digital signal from the memory circuit 701 is directly inputted to the digital-to-analog converter to form an analog signal. As shown in Fig. 16, the signal undergoes a change in accordance with the quantizing error during a voice interval, thus generating a noise cacophonous to the ear. In the quantizing noise remover according to the present embodiment, in contrast, as shown by 1601b in Fig. 16, upon the lapse of a predetermined time t considered to be a voice interval, a digital signal corresponding to "0" level is forcibly subjected to digital-to-analog conversion by the AND gates 1510 to 151n, and therefore the above-mentioned noise continues to be outputted until the arrival of the next "0"-level audio signal free of the noise. The predetermined time length t is very short and ranges from about 0.5 ms to 20 ms, and therefore the quantizing noise generated during this period is not offensive to the ear.

The quantizing noise remover 1500 according to the present embodiment is not only used with the player 101 as described above but also finds wide applications as various digital audio processors such as a digital audio tape recorder processing a digital audio signal.

Fig. 17 is a circuit diagram showing an embodiment of a security circuit used with a digital signal selling system according to the present invention.

In selling an audio signal, etc. in digital form as a commodity, it is important to prevent it from being easily duplicated in order to improve the commercial value thereof. For this purpose, a first method is to add the function of permitting only a specified person to perform the substantial playback operation of the digital signal. In a second method, upon transfer to the player 101 of a digital signal sold in the digital signal selling system according to the above-mentioned embodiment, the signal conversion described below is effected within the player 101 as a function to prevent read duplication.

In order to permit only a specified person to perform the playback operation or to duplicate, the read output section of the memory circuit 701 is provided with EOR gates 1700 to 170n controlled by a password check signal. These EOR gates 1700 to 170n may be either provided as parts corresponding to all bits of the read signals D0 to Dn or only for one or a plurality of bits including at least the most significant bit with equal effect.

The input data terminal of the memory circuit 701 is supplied directly with a digital signal transferred from the terminal device 100 (information server). In the case of using a semiconductor memory with the input and output of the memory circuit 701 shared with each other, the EOR gates 1700 to 170n are inserted in the read signal route of the signal bus connecting the data terminal of the memory. The digital signal is read out of the memory circuit 701 by an address signal generated by the address counter 702 receiving an address update pulse.

The password described above is set in advance in the player 101 by a switch, ROM, etc. This password is notified to the purchaser at the time of purchase of the player 101 by him. As a result, the password is set at the time of reproducing the digital signal by the player 101. When the password registered by a comparator or the like not shown coincides with the password inputted, a password judging signal is reduced to "0". The EOR gates thus output a "0" coincidence signal when "0" coinciding with "0" is inputted thereto. When "1" signal not coincidental with "0" is inputted, on the other hand, a "1" noncoincidence signal is outputted. In this way, when the password judging signal is "0", the EOR gates 1700 to 170n output an input digital signal in its direct form.

When it is judged by a comparator, etc. not shown that a registered password fails to coincide with the input password, by contrast, the password judging signal of "1" is outputted. As a result, the EOR gates output a "0" coincidence signal when a "1" signal coinciding with "1" is inputted thereto, and a "1" noncoincidence signal when "0" not coinciding with "1" is inputted thereto. In this fashion, when the password judging signal is "1", the EOR gates 1700 to 170n output an input digital signal in an inverted form. When the EOR gates 1700 to 170n are inserted for the digital signals of all the bits as explained above, all the bits are inverted when the passwords fail to coincide with each other, so that the resulting audio signal with inverted bits, which is meaningless if converted into an analog signal, assures the confidentiality of information. Also, a password is required even when taking a copy, or, in other words, even when the data is outputted outside from the memory circuit 701, thus preventing an easy duplication.

Some information such as news or traffic data are too small in importance to protect. In such a case, the password may be made null and void by use of the ID code 1308 mentioned above. In other words, the system may be arranged to perform the above-mentioned security operation on condition of coincidence of the password, only when information protection is required by the ID code 1308. By doing so, the seller may designate an item requiring security. Also, a call received by the automatic answering telephone set may be of such a nature that one wants to keep it private. In such a case, an arrangement may be made to designate security mode by the ID code 1308 to assure protection by the terminal device 100. In any way, the operating trouble is minimized by making such as arrangement as to require a password input only when true information protection is assured by the ID code 1308.

Fig. 18 is a circuit diagram showing another embodiment of the security circuit used with the digital signal selling system according to this embodiment. According to this embodiment, a security circuit using

one of the signals D0 to Dn by a selection signal formed by a decoder 2202.

In the case where the digital signals D0 to Dn are eight bits, a random number generator 2204 generates a 3-bit random number (0 to 7 in decimal notation), which is supplied to the input terminal B of the multiplexer 2203. The other input terminal A of the multiplexer 2203 is supplied with a 3-bit binary signal (000) designating the decimal zero corresponding to the output bit D0. The selection terminal S of the multiplexer 2203 is supplied with a password judging signal. The password judging signal becomes a logic zero when the password is coincidental, so that the signal of the input A of the multiplexer 2203 is sent from the output Y.

As described above, when the password is coincidental, the decimal zero corresponding to the output bit D0 is inputted to the decoder 2202 through the multiplexer 2203, and therefore a selection signal of the input bit D0 is formed and supplied to the selector 2201 by the decoder 2202. When the password is incoincident, on the other hand, the 3-bit signal generated by the random number generator 2204 is selected and inputted to the decoder 2202. As a result, the decoder 2202 decodes a 3-bit signal and forms one selection signal from the 8-bit input signals D0 to Dn. The probability of the input signal D0 being selected is 1/8. since a similar circuit is provided also for the remaining 7-bit output signals, the probability of the input signals D0 to Dn being outputted in their direct form even when the password is incoincidental is as small as $1/(8 \times 8 \times 8 \times 8 \times 8 \times 8 \times 8 \times 8) = 1/16777216$, thus making information protection possible. The feature of this circuit lies in that since the random number generator 2204 makes the combination of bit exchange different in each case, it is substantially impossible to decode true data from the bit train outputted.

Now, explanation will be made about an embodiment of the function of preventing the digital signal stored in the memory circuit 701 of the player 101 from being read rightly from outside. Normally, the data terminal (D in Fig. 4) of the player 101 has the input and output thereof shared with each other. And an output enable signal is supplied for keeping the data terminal in output state. In other words, although the logic level is not specifically limited, the player 101 has the data terminal thereof kept in output state only when the output enable signal is valid (logic "1" according to the present invention). As a result, the duplication preventing circuit is inserted, though not specifically limited, in the part related to the data read route.

Fig. 23 is a circuit diagram showing an embodiment of the security circuit suitable for duplication prevention used with a digital signal selling system according to the present invention. In order to allow a specified person to duplicate, the read output section of the memory circuit 701 has an AND gate 2301 for controlling an output enable signal OE by a password judging signal and buffers 23000 to 2300n with the outputs thereof controlled by the output enable signal OE. These buffers 23000 to 2300n are adapted to maintain the outputs thereof in high impedance state as long as the control input is not logic "1". Normally, these buffers 23000 to 2300n are provided as parts corresponding to all the bits of the read signals D0 to Dn.

The input data terminal of the memory circuit 701 is supplied directly with a digital signal transferred from the terminal device 100. In the case of using a semiconductor memory with the input and output of the memory circuit 701 shared with each other, the buffers 23000 to 2300n are inserted on the read signal route of the signal bus connected with the data terminal of the memory circuit. A digital signal is read from the memory circuit 701 by an address signal generated by the address counter 703 not shown. Also, the output enable signal OE is inputted to the AND gate 2301 together with a password judging signal, which is controlled by the password judging signal inverted by the inverter 2302.

This password is set in advance in the player 101 by switch, ROM, etc., and is notified to the purchaser at the time of purchase of the player 101. As a result, when a stored digital signal is read out by the player 101, the above-mentioned password is set. When a password registered by a comparator, etc. not shown coincides with an inputted password, the password judging signal is reduced to logic "0", and after being inverted in the inverter 2302, is inputted to the AND gate 2301. Thus the AND gate 2301 outputs a logic "0" signal when the output enable signal OE is logic "0", and a logic "1" signal when the output enable signal OE is logic "0". In this way, when the password judging signal is logic "0", the buffers 23000 to 2300n are controllable by the output enable signal OE.

In contrast, when the password registered by a comparator, etc. not shown is judged to coincide with the inputted one, the password judging signal is made logic "1", and after being inverted in the inverter 2302, is inputted to the AND gate 2301. As a result, the AND gate 2301 outputs a logic "0" signal regardless of whether the output enable signal OE is logic "0" or "1". In this way, when the password judging signal is logic "1", the outputs of the buffers 23000 to 2300n are maintained at high impedance state regardless of the output enable signal OE. As a result, an easy duplication is prevented by requiring a password when the data of the memory circuit 701 is outputted outside.

Fig. 24 is a circuit diagram showing another embodiment of the security circuit suitable for duplication prevention used with a digital signal selling system according to the present invention. In this embodiment, the read output section of the memory circuit 701 has AND gates 24010 to 2401n for controlling

where the player user is an aged person or the like, on the other hand, it is considered effective to add the slow playback function in view of the fact that it takes some time before the language is understood.

In an analog-type recording system such as the conventional cassette tape recorder, the tape speed may be changed to assure slow or fast playback by changing the playback time as compared with the recording time. When the tape speed is changed this way, however, the pitch (frequency) is also undesirably changed, resulting in the loss of fidelity to the original sound, thereby making it very hard to listen to.

On the other hand, the playback speed may be changed without changing the pitch by the use of the signal processing technique using a digital signal processor or the like. In such a system, however, the configuration is complicated with an increased power consumption, with the result that it cannot be mounted on the portable player and at the same time the cost is very high. Further, such a system is effective only for voice and the reproduction of a music program is difficult.

According to the present embodiment, the voice interval contained in the audio information is utilized in such a manner that the voice interval is shortened or substantially deleted for fast playback and enlarged or extended for slow playback. By employing this system, a high sound quality is maintained since the pitch of the original sound remains unchanged in both fast and slow playbacks. In addition, this configuration, as described later, is realizable with a comparatively simple combination of logic circuits without using any expensive, complicated devices like the digital signal processor, thus making possible a system low in price and small in size.

The embodiment of Fig. 30 concerns a case in which the system is mounted on the player 101 of the digital signal selling system.

The digital audio signal read from the memory circuit 701 is inputted to a digital-to-analog converter 707 on the one hand and to a voice interval detector 3002 on the other hand. The voice interval detector 3002 may be made up of a circuit similar to the one used in the quantizing noise neglector 1500 in the embodiment of Fig. 15. In the case where the quantizing noise remover 1500 is also incorporated, the voice interval detector 3002 may be shared therewith in operation. The output signal of the voice interval detector 3002 is inputted to a fast/slow playback circuit 3003. The fast or slow playback is designated for the fast/slow playback circuit 3003 under the control signals of modes 1 and 2. This fast/slow playback circuit 3003 controls the operation of the address counter 703 for forming a read address signal of the memory circuit 701 in response to a mode signal. When the fast playback is designated by mode 1, for example, the clock frequency is increased beyond normal level to increase the speed of reading the memory circuit 701 during a voice interval which may be detected, thus substantially shortening the voice interval to achieve fast playback.

Assume that the slow playback is designated by mode 2. When a voice interval is detected, the clock frequency is decreased below normal level or suspended for a predetermined length of time thereby to enlarge or extend the read time for the memory circuit 701 during the voice interval, thus achieving the slow playback. The output signal of the address counter 703 is inputted to the memory circuit 701 through the multiplexer 702. When a digital signal is written into the memory circuit 701, the multiplexer 702 causes an external address signal to be inputted to the memory circuit 701, while when a digital signal stored in the memory circuit is read, i.e., at the time of playback of the digital signal, the address signal generated by the address counter 703 is inputted to the memory circuit 701.

Fig. 31 is a block diagram showing a specific embodiment of the fast playback circuit.

According to this embodiment, the output signal of the voice interval detector 3002 is supplied through an inverter 3102 to an AND gate 3103. This AND gate 3103 is for inputting the digital signal from the memory circuit 701 to a digital-to-analog converter 707, and is configured the same way as the quantizing noise remover 1500. Specifically, this embodiment is intended to achieve the fast playback while at the same time eliminating the quantizing noises during the same interval.

The output signal of the voice interval detector 3002 is inputted to the control terminal S of the multiplexer 3101. The mutiplexer 3101 is adapted to input two clock pulses CK1 and CK2 selectively to the address counter 703 in accordance with the output signal of the voice interval detector 300 inputted to the control terminal S. The clock pulse CK1, for example, is one corresponding normally to playback, and is adapted to have a frequency corresponding to the sampling rate of the digital signal. The clock pulse CK2, by contrast, is used for fast playback and has a frequency about ten times higher than the clock pulse CK1.

As long as the fast playback is designated, upon judgement of a voice interval by the voice interval detector 3002, the output signal is raised to high level (logic "1"). In response to this, the output signal of the inverter 3103 is reduced to low level (logic "0"), and the AND gate 3103 is closed. In the case of a digital signal of 2' complement binary code as mentioned above, therefore, the digital signal inputted to the digital-to-analog converter 707 during a voice interval is forcibly made to correspond to the "0" level. Also, with the rise of the output signal of the voice interval detector 3002 to high level, the multiplexer 3101 inputs the clock CK2 instead of the clock CK1 to the address counter 703. As a result, the address counter 703 up-

is substantially restarted. At the same time, the AND gate 3208 is opened, and the digital signal thus read is supplied to the digital-to-analog converter 707. Thus the audio signal is outputted again. In this configuration, the extension of the voice interval is proportional to the voice interval of the original sound. Therefore, a conversation or lecture is accordingly increased in the length of interval and is made less offensive to the ear.

When a voice interval is counted, the quantizing noise is outputted as described above. For removing this quantizing noise generated during the counting of a voice interval, a method is by inverting the output signal of the voice interval detector 3002 through an inverter to control the AND gate 3208. In such a case, a three-input AND gate is used as the AND gate 3208. When a voice interval is counted, the quantizing noise is eliminated by the output signal of the voice interval detector 3002 added as above, and by the output signal Q of the flip-flop 3201 while the voice interval is enlarged subsequently, as described above.

Fig. 33 shows waveforms of operation associated with the fast playback circuit of Fig. 31. The voice intervals 3303 (Tm1) and 3304 (Tm2) of the original signal 3301 can be removed substantially by switching the clock pulses supplied to the address counter 703 during such intervals, and therefore the fast playback is made possible without changing the pitch (frequency) of the audio signal, i.e., without deteriorating the sound quality of the audio signal.

Fig. 34 shows waveforms of operation associated with the slow playback circuit of Fig. 32. Since the voice intervals 3303 (Tm1) and 3304 (Tm2) of the original signal are enlarged to n times as large by suspending the operation of the address counter 703 during the same intervals, the slow playback is realized without changing the pitch (frequency) of the audio signal, i.e., without deteriorating the sound quality of the audio signal.

Fig. 35 is a block diagram showing another embodiment of the fast playback circuit according to the present invention.

In this embodiment, the address-generating operation is directly switched by using an adder 3501 with the address counter 3503 in order to achieve fast playback. Specifically, the address counter 3503 includes the adder 3501 and a register 3503 for receiving a sum output A+B thereof. The output signal Q of the register 3503 is fed back to the sum input A on the one hand, and is inputted to multiplexer 702 as a read address of the memory circuit 701 on the other hand.

The other input B of the adder 3501 is supplied selectively with 1 and a positive integer M through the multiplexer 3504. The control terminal S of the multiplexer 3504 is supplied with an output signal of the voice interval detector 3002. The output signal of the voice interval detector 3002 is supplied also to the AND gate 3505 for eliminating the quantizing noise through the inverter 3209 as in the aforementioned embodiment.

When a voice interval is detected by the voice interval detector 3002, the multiplexer 3504 selects M in place of 1, and transmits it to the adder 3501. As a result, before entering a voice interval, the adder 3501 performs the counting operation by adding +1 to the address signal formed by the register 3502 and generating the next address signal. When a voice interval is entered as mentioned above, the multiplexer 3504 inputs M to the adder 3501. As a result, the adder 3501 adds +M to the address signal formed by the register 3502 to generate an address signal skipped by M addresses. Thus the address-updating operation during a voice interval is equivalently increased in speed, thereby substantially eliminating the voice interval as in the aforementioned embodiments.

Fig. 36 is a block diagram showing another specific embodiment of the slow playback circuit according to the present invention.

In this embodiment, a clock pulse CK4 is prepared for slow playback. Specifically, in contrast to the fast playback circuit shown in Fig. 31, a slow clock pulse CK4 is prepared for slow playback, so that when a voice interval is started, the multiplexer 3601 is switched to select the slow playback clock pulse CK4 in place of normal clock pulse CK1. When the frequency of the clock pulse CK4 is reduced to 1/N in comparison with that of the clock pulse CK1, the operation of the address counter 703 is decreased by a factor of N, thereby enlarging the voice interval equivalently by a factor of N.

In this embodiment, which can be configured with a circuit similar to Fig. 31, the input B of a multiplexer 3601 may be selectively supplied with the clock pulse CK2 in fast playback mode and the clock pulse CK4 in slow playback mode respectively through a similar multiplexer or an appropriate switching circuit. In this way, both the fast and slow playback are made possible.

Fig. 37 is a block diagram showing another specific embodiment of a slow playback circuit according to the present invention.

In slow playback mode, the user like an aged person feels more convenient to hear as described above. If a comparatively long voice interval is enlarged or extended, however, the sound becomes difficult to hear. In view of this fact, the embodiment under consideration has added thereto the function of imposing a certain limitation on the enlargement or extension of a voice interval in slow playback mode.

According to this embodiment, a circuit described below is added as a basis of the slow playback circuit shown in Fig. 32. The output signal Q of the voice interval counter 3202 is increased N times as large by a multiplier 3703. The N-fold multiplier output is supplied to an input A of a multiplexer 3705 and an input A of a comparator 3706. The output signal Q of the

interval data 4102 (MK), the voice intervals 3303, 3304 are replaced by information of several bytes, and therefore the voice intervals 3303, 3304 contained in the digital signal before analog conversion are substantially removed. As a consequence, the memory capacity required for storing digital signals can be reduced to about 1/2 to 2/3 or by the proportion which the voice interval represents of the whole time length. In the case where a data is compressed in this way, utilization of the voice interval data 4102 (MK) makes slow or fast playback possible by enlarging or compressing the same signal selectively. This data compression may basically use a fast playback controller as described above. Although the fast playback controller outputs a "0" level signal in order to remove the quantizing noise during a voice interval, the voice interval data 4102 (MK) may alternatively be inserted with equal effect.

Fig. 42 is a pattern diagram showing an embodiment of the voice interval data 4102 (MK).

The voice interval data 4102 (MK) includes a voice interval mark 4203 and a voice interval time data 4204. A combination of bit patterns unavailable for a normal digital signal is selected as the voice interval mark 4203. According to this embodiment, when the digital signal is a 2' complement binary code, a combination of a positive maximum value 4201 (01111111) and a negative maximum value 4202 (1000000) is used. A normal audio signal does not change from a positive to a negative maximum value, and therefore this combination is used as a voice interval mark. The voice interval mark 4203 may alternatively be a combination of two, three or four bytes, unlike in the above-mentioned combination.

The voice interval time data 4204, though not specifically limited, may have two bytes. In order to meet the requirement of a longer voice interval, however, three or four bytes may be used for the voice interval time data 4204.

Fig. 43 is a block diagram showing an embodiment of a digital signal playback controller including the function of fast and slow playback modes against the digital signal compressed in the manner described above.

The address counter 703 is supplied with an address counter clock ADCK through an AND gate 4311. When the voice interval data 4102 (MK) includes a two-byte voice interval mark 4203 and a two-byte voice interval time data as mentioned above, the read signal for the memory circuit 701 is outputted through four-stage shift registers 4301a to 4301d correspondingly thereto. These shift registers 4301a to 4301d are supplied with a data shift clock DSCK through an AND gate 4312.

The outputs A and B of the shift registers 4301d, 4301c are inputted to a voice interval mark detector 4303. The mark detector 4303 compares the bit patterns of the signals A and B to determine whether they coincide with the positive maximum value 4201 (01111111) and the negative maximum value 4202 (10000000) respectively. The detection signal from the voice interval mark detector 4303 is used for setting the flip-flops 4308 and 4309.

The outputs C and D of the shift registers 4301b and 4301a are supplied to an input A of the comparator 4304. The other input B of the comparator 4304 is supplied with the output signal of the voice interval counter 4305. The output signal of the comparator 4304 is supplied through the AND gate 4315 to the reset terminal R of the voice interval counter 4305 and the input CK of the repeat counter 4306 used for extending a voice interval. The output Q of the repeat counter 4306 is compared with an extension factor N at the comparator 4307.

The output Q of the flip-flop 4309 is supplied through the inverter 4314 to the OR gate 4315 and the AND gates 4311, 4312. Upon detection of the voice interval mark 4203, therefore, the operation of the address counter 703 and the shifting operation of the shift register 4301a to 4302d are stopped, thereby holding the voice interval data 4102 (MK) in the shift registers 4301a to 4301d. With the stoppage of operation of the address counter 703, the memory circuit 701 has the reading operation thereof suspended. The output signal of the comparator 4307 is supplied to the reset terminal R of the flip-flop 4309 and the repeat counter 4306.

The output Q of the flip-flop 4308 is set as a voice interval flag FLG and makes up a control signal for the AND gate 4310 through the inverter 4313. Upon detection of a voice interval mark this way, the AND gate 4310 is immediately closed, thereby preventing the positive maximum value 4201, the negative maximum value 4202 and the following time data 4204 from being outputted erroneously as an audio signal. Especially when the positive and negative maximum values are used as a voice interval mark 4203, a large pulse-like noise would be caused if such values are outputted directly in their own forms.

The voice interval flag of the flip-flop 4308 is fed back through four-stage D-type flip-flops 4302a to 4302d as a reset signal for the flip-flop 4308. These flip-flops 4302a to 4302d, as explained below, are used to transmit the voice interval by the same data shift clock as the shift registers 4301a to 4301d, thereby detecting a time period, at the and of the voice interval, in which the voice interval data 4102 (MK) including the voice interval mark 4203 and the time data 4204 thus far held in the shift-registers 4301a to 4301d is swept out. When it is judged by the flip-flops 4302a to 4302d that the voice interval has been ended, the flip-flop 4308 is reset.

After the flip-flop 4309 is set upon detection of the voice interval mark 4203, the reset state of the voice counter 4305 is cancelled through the inverter 4314. The voice interval counter 4305 starts the

data compression and expansion.

Fig. 44 is a block diagram showing an embodiment of a data converter configured by a data conversion system according to the present invention.

The data converter according to this embodiment, though not specifically limited, is for converting an analog signal into a 16-bit digital signal and is intended for a circuit for compressing and outputting the digital data as an 8-bit digital data.

The analog signal Vin is inputted to the analog-to-digital converter 4401 and is converted into a digital data of n bits (16 bits, for example, as mentioned above). This embodiment uses a circuit described below for compressing the digitally-converted 16-bit data into a data of m bits (8 bits, for example).

One of the inputs of the subtractor 4402 is supplied with the 16-bit data D1 digitally converted as above. The other input of the subtractor 4402 is supplied with a 16-bit data D2 stored in the register 4406. The 16-bit data D2 stored in the register 4406 is assumed to be an immediately preceding sampling data as described later. The subtractor 4402 subtracts the immediately preceding sampling data D2 stored in the register 4406 from the input data D1 digitally converted, and outputs the difference (D1 -D2) therebetween. The difference data D3 is supplied to an input B of the comparator 4403. The other input A of the comparator 4403 is supplied with a data D4 corresponding to the maximum value of an 8-bit data to be compressed. This data D4 is comprised of 16 bits of 0000000011111111 (255 in decimal notation) as shown with all the least significant eight bits (m) as 1.

The comparator 4403 compares the data D3 and D4 supplied to the input terminals A and B, and when B is larger than A (D3 > D4), forms a high-level output signal, while when A is larger than B generates a low-level output signal. The output signal of the comparator 4403 is used as a selection signal.

An input A of the selector 4404 is supplied with an 8-bit maximum value data d4 to be compressed (11111111), and the input B with a data d3 representing the least significant eight bits of the difference data D3. The selector 4404 selects and outputs the maximum value data d4 of the input A when the output signal of the comparator 4403 is at high level, i.e., when the substraction data D3 is larger than D4, and the data d3 of the least significant eight bits of the substraction output supplied to the input B when the output signal of the comparator 4403 is at low level, i.e, when the subtraction data D3 is smaller than D4.

The output signal d5 of the selector 4404, though not specifically limited, is stored in the memory 4408, and read and outputted as a compressed 8-bit digital data Dout. The output signal d5 of the selector 4404 is supplied to one of the inputs of the adder 4405. The other input of the adder 4405 is supplied with the output data D2 of the register 4406. As a result, the adder 4405 adds the compressed data d5 outputted from the selector to the immediately preceding sampling data D2 stored in the register 4406, so that the sampling data D2' updated and assumed to be immediately preceding to the next input data D1 is formed and stored in the register 4406. In this way, the accumulation error is prevented by generating the next sampling data by the register 4406 and the adder 4405.

Subsequently, the 16-bit (n-bit) input data D1 is converted into an 8-bit (m-bit) compressed data d5 by repeating similar processes.

Fig. 45 shows waveforms for explaining the operation of analog-to-digital conversion accompanied by the data compression described above.

At the time of data compression, the register 4406 is cleared of data (0000000000000000). As a result, when an analog signal rises sharply as shown, the progressive adding operation of the least significant 8-bit maximum value would fail to follow an input digital signal. Once the difference between the input digital signal and the immediately preceding sampling data is reduced below the maximum value of the compressed data, however, it is possible to obtain a compressed data faithfully corresponding to the input signal change. As for an acoustic signal which has an amplitude and a frequency distribution changing comparatively gently with time, data compression is possible with a fidelity posing no practical problem.

Fig. 46 is a block diagram showing another embodiment of a data converter in a data conversion system according to the present invention. This embodiment is intended for a circuit in which a data compressed into m bits (eight bits, for example) as in the aforementioned embodiment is extended into an n-bit (16-bit) data and at the same time is outputted by being converted into an analog signal.

The data Din compressed by a data compressor as shown in Fig. 44, though not specifically limited, in transferred and stored in a memory 4601 of Fig. 46 from the memory 4408 in Fig. 44. In some cases, the memory 4408 in Fig. 44 and the memory 4601 in Fig. 46 are used in common with each other. The data d5 read out of the memory 4601 is supplied to an input of the adder 4602. The other input of the adder 4602 is supplied with an n-bit data D6 stored in the register 4603. The adder 4602 forms a data D7 by adding the data d5 to D6. This data D7, though not specifically limited, is inputted to the register 4603. The data D6 outputted from the register 4603 and extended is inputted to the digital-to-analog converter 4604 to form a demodulated analog signal Vout.

The operation of the data extender will be explained. At the time of starting the data extending operation, the register 4603 is cleared as in the aforementioned case. The compressed data d5 read out of the memory 4601 is added to an immediately preceding n-bit data D6 of the register 4603 each time of reading, and is stored in the register 4603 as expand-

register 4701 is larger than the count Q of the counter 4703 (A > B). This comparator 4702 forms a low-level signal when the count output Q of the counter 4703 increases beyond the data line input digital signal Din (A < B). This embodiment including a repeat counter 4704 is such that an output pulse corresponding to the next input digital signal is not immediately formed as in the conventional systems but a pulse having a pulse width corresponding to the one input digital signal Din is subjected to repeated conversions in the number of J as designated by the repeat counter 4704.

Fig. 48 shows waveforms for explaining an example of operation of the digital-to-analog converter described above.

In the case where the digital input signal Din has eight bits, for instance, the period of the 10-MHz clock pulse CK is 0.1 μs, and therefore when an 8-bit counter is used, one period is 25.6 μs. As a result, when the input digital signal is a decimal 1, a high-level pulse is outputted during the first 0.1 μs and a low-level pulse during the remaining 25.5 μs. When the input digital signal is decimal 10, on the other hand, a high-level signal is outputted only during the first 1 μs, and a low-level pulse during the remaining 24.6 μs. In similar fashion, when the input digital signal is 100 in decimal notation, a high-level signal is outputted only during the first 10 μs, and a low-level pulse during the remaining 15.6 μs. When the input digital signal assumes 255 which is the maximum decimal value, a high-level pulse is outputted during the first 25.5 μs and a low-level pulse during the remaining 0.1 μs.

Fig. 48 shows a case in which the number of repetitions J is 4. When an output signal converted into a pulse width is outputted four times repeatedly as mentioned above, a conversion output signal EOC corresponding to an input digital signal Din is outputted. In this way, in the case of four repetitions, the conversion time for forming four pulse width modulated outputs within the period of fetching the data read from the memory circuit 701 in the player 101 is 25.6 x 4 = 102.4 μs, thus making possible a conversion frequency of about 10 kHz. This is most suitable for reproduction of a news program, a conversation, a lecture or speech. In reproducing a music program of high sound quality, high frequencies up to about 20 kHz can be reproduced in the process of four repetitions If the frequency of the clock pulse CK is 20 MHz. If the number of repetitions is reduced by two while keeping the clock pulse CK at 10 MHz, on the other hand, high frequencies up to 20 kHz can be reproduced in similar fashion. In this way, a combination of the frequency of the clock pulse CK and the number of repetitions is matched with the sampling period of the input digital signal.

Incidentally, when a digital signal is inputted again in synchronism with a strobe STB in response to the conversion output signal EOC, a corresponding analolg-to-digital conversion is effected in similar manner.

The pulse width modulated signal outputted from the comparator 4702 is smoothed by a low-pass filter 4708 including a resistor 4706 and a capacitor 4707, and is outputted as an analog signal Dout. According to the present embodiment, such pulse width modulated signals are outputted in a plurality of numbers. As a result, even when the response is increased by setting the time constant due to the resistor 4706 and the capacitor 4707 to small value for improving the sound quality of the output signal, the ripple component is kept to minimum.

In the circuit according to the present embodiment which has the whole circuit capable of being configured of digital circuits, as compared with a case in which a digital circuit may be mixed with an analog circuit, the processes are simplified and the system may be configured of a CMOS integrated circuit or the like which is simple in the process and low in consumption.

Fig. 49 is a block diagram showing another embodiment of the digital-to-analog converter according to the present invention. The digital-to-analog converter according to the present embodiment is intended for simplifying the circuits.

According to the present embodiment, the comparator 4702 shown in Fig. 47 is done without and a pulse width modulated signal is formed corresponding to the digital signal by a down counter 4901 and flip-flop 4902. Specifically, the down counter 4901 has set therein an input digital signal Din in synchronism with a strobe. As a result, the output signal Q of the flip-flop 4902 changes to high level, and the down counter 4901 starts counting the clock by the strobe mentioned above. The down counter 4901 outputs a borrow signal BO and resets the flip-flop 4902 when the count thereof becomes zero. This borrow signal BO is sent to the input side as an end-of-conversion signal.

The flip-flop 4902 is set simultaneously with the starting of counting the digital signal, and is reset when the clock corresponding to the digital signal is counted. As a result, the output signal Q of the flip-flop 4902 is converted into a pulse width modulated signal corresponding to the input digital signal.

A signal source inserted in the input side of the digital-to-analog converter according to this embodiment outputs a digital signal and a strobe corresponding to a predetermined sampling period like the memory circuit 701. As a result, the next digital signal is sent from the signal source not immediately after the conversion-over signal EOC is sent out, but on condition that a digital signal and a strobe are sent out in synchronism with the sampling period. Thus it is possible to produce a pulse width modulated signal corresponding to an input digital signal of a predetermined period by the setting operation synchronous

the borrow output BO of the down-counter 5001. This AND gate 5006 inhibits the set signal FR of the flip-flop 5003 from the controller 5004. In this way, when the digital signal Din is decimal 0, no pulse is outputted from the flip-flop 5003. When the digital signal Din is 1 or more, in contrast, a pulse having a pulse width corresponding to the output Q of the flip-flop 5003 is outputted. The output signal thus subjected to pulse width modulation is smoothed by a low-pass filter 5007 thereby to form an analog signal Vout.

The up-counter 5002 continues the counting operation, and outputs a carry signal CAR when the count reaches the maximum. The controller 5004, upon receipt of the carry signal CAR, changes the conversion-over signal EOC to logic "0" thereby to end the whole series of the converting operation. Upon completion of the conversion, the next digital signal is inputted. Specifically, in the case where the up-counter 5002 is provided as described above, an address signal is generated by the end-of-conversion signal EOC following a digital-to-analog conversion to read the next input digital signal.

As explained above, when the input digital signal and the strobe are inputted, the above-mentioned operation is repeated to form an analog signal Vout corresponding to the input digital signal Din. The controller 5004 raises the end-of-conversion signal EOC to high level and notices the fact to an external circuit during the conversion process, and continues the conversion without answering to a strobe ignoring the notice.

In reducing the ripple component of the analog conversion output Vout, a repeat counter or the like is provided for each conversion start signal like a strobe to repeat a designated number of digital-to-analog conversions as mentioned above. In the case where no input of a digital signal Din is assured during this repetition, a register should be provided to fetch an input digital signal in the same manner as described above.

The embodiments explained with reference to Figs. 47 to 50 may be applied widely as a signal converter for converting a digital signal into a pulse width modulated signal as well as to a digital-to-analog converter.

Fig. 51 is a basic block diagram showing an embodiment of a switch input circuit for the player 101 used with the digital information system described above.

As described already, the player 101 is reduced in size and thickness so as to be compatible with an IC memory card or the like. As a result, it is considered important to reduce the switches or the like for designating an operation mode. In view of this, according to this embodiment, signals 5103-1 to 5103-n for designating the states 1 to state n are formed by a state controller 5102 receiving an on/off signal of a key switch 5101. By doing so, a package of switches can be accommodated in a limited space of the small and thin player 101 as described above.

Fig. 52 is a block diagram for explaining an embodiment of a specific configuration of a state controller.

According to this embodiment, an on time of the switch 5101 is judged by the state controller 5102. The state controller 5102 forms a signal 5201-1 for turning on state A unconditionally once the switch is turned on regardless of the on time T of the switch 5101. The state controller 5102 forms a signal 5201-2 for turning on state B when the on time T of the switch 5101 is smaller than a predetermined time length M (M > T). The state controller 5102 further forms a signal 5101-3 for turning on state C when the on time T of the switch 5101 is judged to be larger than a predetermined time length M (M ≦ T). By combining the signals 5101-1 to 5101-3 representing these three states A to C, the playback control operation mentioned below is realized.

Fig. 52 is a schematic diagram for explaining this operating mode.

The player 101 is set in a stop state immediately after power is thrown in. In this state 5302, assume that the switch 5101 is turned on. A signal 5301a indicating an unconditional state A regardless of the on time T is formed to set the player 101 in playback state 5303. In this playback state 5303, it is necessary to select one of two choices, one to change to a pause state 5305 and the other to return to the stop state 5302. When the switch 5101 is turned on again, the signal 5301b indicating the state A is formed and the time judgement 5304 is started, thereby judging the time T turned on. If the judgement is a signal 5301c indicating the state B, the player 101 is set to the pause 5305. If the judgement is a signal 5301e indicating the state C, on the other hand, the player 101 is returned to the stop state 5302. In the stop state 5305, the only meaningful operation is to return to the playback state 5303, and therefore the switch 5101 is only turned on so that the playback state 5303 is restored by the signal 5301d indicating the state A as described above.

In the case where a plurality of types of operation are designated by a switch, the disadvantage is a complicated operating procedure. According to the embodiment under consideration, in order to enable the user to master the operating procedure easily, light-emitting diodes or liquid crystal display devices are provided as elements corresponding to the stop state 5302, playback state 5303 and the pause state 5305 shown in Fig. 51. These elements are lit in accordance with the present state, and are combined with arrows shown in Fig. 51 thereby to indicate a state into which a change is possible by the input of the states A to C. This indication is effected only for a predetermined time of switching operation to save power consumption in the case where a light-emitting

operation, thus providing a system very easy to operate. Another feature of this embodiment lies in that since the block length can be determined exactly as desired, and therefore the data memory 5610 can be utilized without waste very efficiently. This is due to the fact that the performance of a semiconductor memory is fully used taking advantage of the characteristics thereof, and shows an example of effectiveness of the system according to the invention. Although a memory is divided into the data memory 5610 and the block address memory 5601 in this embodiment, they may be arranged as a single memory unit with equal effect.

Fig. 57 is a schematic diagram showing an embodiment of a storage area management system of the memory circuit 701 of the player 101.

In order to assure efficient use of the storage capacity of the memory circuit 701 mounted in the player 101 against a plurality of pieces of information, the memory circuit 701 is divided into a contents area and a data area. The contents area, though not specifically limited, has four contents 5701a to 5704a, capable of storing block addresses BA0 to BA3 respectively. The contents 5701a to 5704a are selected by program select signals PSL1, PSL2 and the like thereby making it possible to write or read the block addresses BA0, BA1, etc.

In the above-described digital information system, the terminal device 100, when connected with the player 101, accesses the contents area and reads an effective block address. As a result, the terminal device 100 is in a position to know a vacant area of the memory circuit 701 of the player 101. When a new digital signal to be received is designated, the block address is stored in the vacant contents area while at the same time storing a digital signal in the vacant area.

If the contents are in short supply or the vacant storage capacity is lacking for the digital signal received, a digital signal that has been already stored and that may be erased by display is selected, and by erasing the particular digital signal, a new digital signal is inputted. In the process, the digital signal that is already stored in the player 101 is also read out, and an address is allocated in such a manner as not to cause any vacancy of storage area in accordance with the storage capacity of the new digital signal.

In Fig. 57, the contents 5701a are addressed by a program access signal PSL1, so that the block address BA0 stored therein is read and set in the address counter 703. Assuming that the block address BA0 set in the address counter 703 is the data block 5701d of the head address of the data area as shown by solid line, for example, the ID code 5701i at the head of the block and subsequent addresses start to be read sequentially. The last address of the data, though not specifically specified, has an end mark 5701e stored therein, by detection of which the reading process is ended. In this configuration, it is sufficient to store only the head address in the contents and therefore the address information can be reduced.

Also, the contents 5702 are accessed by the program select signal PSL2, and the block address BA2 stored therein is read and set in the address counter 703. In the case where the block address set in the address counter 703 makes up an intermediate block as shown by dotted line, for instance, the addresses having the head ID code 5702i of the particular block and subsequent addresses start to be read in that order. The last address of the data 5702d has the end mark 5702e stored therein in the manner similar to the preceding case, and the reading process is ended upon detection of the end mark 5702e.

Assume that some data blocks storing the above-mentioned two types of program are vacated by erasure of a digital signal corresponding to the contents 5701a or otherwise, for example. The terminal device 100 changes the block address BA2 of the contents 5702a to an address of the end mark 5701e of the data area corresponding to the contents 5701a, while at the same time writing a corresponding digital signal. By doing so, a digital signal corresponding to the program newly received is usable successively for the remaining vacant areas.

The player 101 can be connected with the terminal device 100 so that the contents area and the data area may be cleared and a new digital signal may be stored. In such a case, desired programs may be reserved by designating a no-erasure on the player 101 side or a no-erasure program as an operation of receiving of a digital signal with the terminal device 100.

Fig. 58 is a schematic diagram showing another embodiment of the storage area management system of the memory circuit 701 of the player 101.

According to this embodiment, a digital signal is stored and managed by a contents memory 5801 and a data memory 5802. The contents memory 5801 can store a maximum of four types of digital signals (programs) including contents 1 to 4, for example. The contents memory 5801 may store only the head address as in the aforementioned embodiment or the contents information in addition to the end address or ID code. This contents information, though not specifically limited, includes character information, so that the program contents can be displayed by characters with a liquid display unit mounted in the player 101.

Each content of the contents memory 5801 and the data area of the data memory 5802 is arranged as desired in such forms as data 2, data 1, data 4 and data 3, for example, from the head address side of the data memory 5802 in the order of storage. Specifically, digital signals are stored in the data memory 5802 in the order of designation.

Fig. 59 is a block diagram showing the essential

plying a selection signal to the multiplexer 6202, a buffer 6204 for connecting the output of the multiplexer 6202 to the memory, a delay line 6206, an address counter 703, a comparator 6203 and a first-in first-out memory 6207. Signals inputted to and outputted from this circuit section include an input data from the terminal device 100, an output data from the memory, a write strobe signal (WE) from the controller to the memory, a RUN signal for indicating "under storage/playback", and two types of memory test pattern data "AA" and "55" as an input. A skip address output and a playback clock input are for skipping the defective portions (defective addresses) of the memory in the process of reading during the playback operation. Immediately after the stored data is changed, the write strobe signal (WE) is inputted with a pulse width of 100 ns (the repetitive frequency of 8 kHz), clears the ternary counter 6201 through the AND gate 6213, and is connected to the control terminal of the buffer 6204 and the WE (write enable) terminal of the memory through the AND gate 6214 and the inverter 6205. The buffer 6204 is a device which is in a high impedance state when the control terminal is at a high level, and the input thereto is reflected in the output terminal thereof only when the control terminal becomes low. The data terminal (DIO) of the memory, on the other hand, outputs the contents of a designated address when the WE terminal is high in level, while when the WE becomes low, the DIO terminal switches to a state capable of accepting a data input, thereby writing the data input of the DIO terminal into a designated address. When the data on the input and output sides of the buffer 6204 immediately after the WE pulse signal has returned to high level (exactly, after the lapse of 50 ns as an access time of the memory), therefore, a normal data should have been written into the memory. If the two data fail to coincide with each other, by contrast, it indicates that a normal data has not been written into the memory. In order to make this judgment, a comparator 6203 is inserted which is so logically configured that the Y output thereof becomes high in level when the contents at the A and B input terminals fail to coincide with each other, and the Y output of this comparator 6203 is supplied as an input to the AND gate 6210. In this configuration, the output of a NOR gate 6205 is also inputted to the pulse delay line 6206 with inverter function. By this delay line 6206, a WE' pulse about 200 ns delayed is outputted and inputted to the other input terminal of the AND gate 6210. In the processes, if the no-coincidence output is at low level, i.e., if the data is normally written into the memory 710, the AND gate 6210 outputs no signal. The ternary counter 6201 is reset at the time of input of a WE pulse thereto (although the clock input CP is also supplied with a pulse, the clearing operation is given priority), and both the QA and QB outputs thereof are at low level with the multiplexer 6202 selecting the pattern "AA" (10101010 sequentially from the seventh power of 2 bits side in hexadecimal or binary notation). Therefore, the data normally written into the memory circuit 701 makes up the first test pattern. Since the QB output (first power of two bits) of the ternary counter 6201 is at low level, this output is raised to high level at the inverter 6216. The AND gate 6211 passes the WE', which passing through the OR gate 6214, counts up the ternary counter 6201 whereby the multiplexer 6202 selects the test pattern "55" (01010101 sequentially from the seventh power of 2 bits side in hexadecimal or binary notation). At the same time, the output of the OR gate 6214 is inputted to the NOR gate 6205 and functions as a write pulse for the memory. Subsequently, when the test pattern "55" or the stored data (input data of the memory) is normally written, the AND gate 6211 is inhibited (since the QB output of the ternary counter 6201 is raised to high level), so that the round loop mentioned above is released. Instead, the WE' pulse is passed through the AND gate 6212, and after counting up the address counter 703, the next write pulse (WE) from the controller is awaited. In the case where the Y output (no-coincidence output) of the comparator 6203 is at high level, i.e., in the case where no normal data has been written into the memory circuit 701, the WE' pulse is passed through the AND gate 6210, and the associated contents of the address counter 703 are written into the first-in first-out memory 6207, while at the same time being inputted to the NOR gate 6205 and the OR gate 6213, thereby repeating once again the same operation as when the WE pulse is inputted. This repetitive operation is continued until a data is normally written into the memory circuit 701 (this repetitive operation requires about 300 ns and the WE input period is about 125 μs. Therefore, the number of repetitions actually allowed is about 400 in the first pattern check, i.e., by generation of an error at the time of writing the pattern "AA", or about 200 in the second pattern check, i.e., by generation of an error at the time of writing the pattern "55".)

According to this embodiment, it is possible to use a semiconductor chip which otherwise might be discarded as a result of inspection when only several bits of large capacity memory cells of megabit class such as four or 16 megabits are defective, and therefore a very inexpensive system is provided. The basic concept here is to conduct inspection before writing and utilize any defective bit by the use of the result of inspection, and various modifications and applications are of course possible by use of this concept. When a defective bit fixed to "1" at the time of writing "1" is detected as a result of inspection, for instance, that bit may be used as "1" as it is.

If the operation of the multiplexer 6202 in Fig. 62 is fixed (QA output of the ternary counter 6201 is fixed to low level and the QB output thereof to high level), a simple self-diagnosis circuit may be configured for

a tiered operating screen. As a result, the convenience to the user is greatly improved. Further, the inverted insertion of the terminal 100 into the player is prevented by appropriate machining. Also, the confirmation switch 6901 is used to prevent erroneous selection of information by the user. After the user confirms the selected information by the testing function mentioned above, the confirmation switch 6901 is depressed to transfer the information instantaneously to the player 101. Further, the display panel 303 is adapted to display, in addition to the normal operation screen, the result of checking the conditions of the cell 710 in the player 101 by the terminal device 100 and a message confirming the insertion of the player.

Furthermore, the terminal device 100 is connected with the player 101 by a connector conforming to the JEIDA or equivalent standard.

The player 101 according to the present embodiment includes a switch for turning on/off a power supply, a switch for designating the slow/fast playback mode, a switch for designating the loudness mode and a pushbutton switch for designating the playback/stop/pause state.

The present invention is not limited to the monochromatic display of the graphic screen or characters on the liquid crystal display unit 303 of the terminal device 100 as according to the present embodiment, but still images or animation may be displayed in color with equal effect.

The effects obtained from the embodiments described above are as follows:

(1) In receiving/delivering a digital signal, a player is directly connected one-to-one with a digital signal source, so that a specified digital signal is directly received and stored in a memory and the digital signal stored independently in the memory is reproduced. In this configuration, the player receives the digital signal and reproduces it independently, so that the value of the digital signal delivered is exhibited in direct form.

(2) As a result of the effect described in (1) above, the digital information as a commodity or the like can be easily processed or produced or the selling system thereof easily set up.

(3) As a result of the effect described in (1) above, the value of the digital signal itself received/delivered is recognized as a commodity or the like, and the player has a simple function of reproducing the particular value. The player thus has a simple configuration and is easily operated by any one.

(4) A digital signal is received from a digital signal source by a terminal device through a communication channel or an appropriate storage medium. A player and a connector are connected with the terminal device to receive/deliver a digital signal, whereby a digital signal selling system is provided for selling a digital signal as a commodity or the like both rationally and at high speed.

(5) A magnetic disk memory having a comparatively large storage capacity is used as a backup memory for the terminal device, and the digital signal large in the amount of receiving/delivery or updated with time is stored in a buffer memory configured of a semiconductor memory accessible at high speed, thus realizing an efficient receiving/delivery of a digital signal.

(6) The terminal device is provided with the microcomputer function to manage the magnetic disk memory or the buffer memory and to exchange a digital signal with the source through a communication channel. Also, the storage area of the memory in the player is managed to permit effective utilization of the memory as well as simplification of the player.

(7) The terminal device is provided with the function of monitoring a part of the digital signal for a predetermined length of time, thereby preventing a selection error or facilitating the selection of an intended digital signal.

(8) The digital signal received/delivered is limited to audio information as a digital audio signal, and therefore the player function is simplified to storage and playback.

(9) The digital signal received/delivered has added thereto an ID code, whereby the playback conditions for the player are automatically designated thereby to receive/deliver a variety of digital signals corresponding to a given information program while at the same time offering an operating ease.

(10) By providing a card-like memory section replaceable from the player body, various RAM, EEPROM or ROM may be used as a memory, thereby increasing the variety of functions.

(11) The outline of the player and the connector are compatible with the existing memory card, whereby an internal memory can be used equivalently to the existing memory card.

(12) As a result of the effects described in (10) and (11) above, the multiple functions and enlarged applications of the player are assured.

(13) The player is provided with a security function for protecting the input and/or output operation of the memory in accordance with a password or a password coincidence detection signal, whereby easy duplication, eavesdropping or the like is prevented thereby increasing the commercial value of a digital signal received/delivered.

(14) As a part of the memory section of the player, a thin card-like memory is replaceably mounted. This makes it possible to enlarge the storage capacity or reproduce a program configured of various ROMs as required, thereby realizing a variety of functions.

(33) Of the functions making up a memory card with a playback mechanism, a digital-to-analog converter, a low-pass filter, an amplifier and a controller except for a memory are integrated as a one-chip integrated circuit, thereby providing a very small device with extremely small power consumption. Also, the mass production is made possible with lower cost.

(34) The above-mentioned memory card with playback function is provided with the function of skipping a defective bit, whereby defective memory chips which have thus far been discarded can be used, thereby providing a device very low in cost.

(35) By providing a player conforming to the JEIDA standard, the compatibility with the existing memory cards is assured.

The present invention which has been explained above with reference to embodiments is not limited to such embodiments. In a digital information system, for example, a digital signal may be not only sold as a commodity but also offered free of charge to a person specified by the player as one of the services offered by securities firms, financial institutions or the like. As an alternative, the whole digital signal may be utilized for receiving/delivery of information required periodically or from time to time by a collective agreement. Also, the digital signal may be in such a form as capable of being transmitted by an audio signal like the data required for language study or memorization for various test objects.

Further, a digital information system mentioned above makes it possible to build a very efficient and timely futuristic media for supplying various information and amenities using a digital audio signal in place of the conventional newspaper, weekly magazines, etc. using prints.

The player may be constructed of a connector connectable with an extending ROM card or RAM card. In such a case, in order to prevent the player itself from being increased in thickness, the ROM or RAM card may be made up of a thin plastic card with a memory chip built therein. The ROM card is convenient for a music program or language learning. The RAM card makes up effective means for enlarging the memory capacity. The RAM card is effective, for example, when receiving a music program or the like with a long performance time.

The configuration, function, etc. of the terminal device and the player used with the digital information system may take various forms of embodiment. The memory built in the player may be a static RAM or a combination of a dynamic RAM and an automatic refresh circuit as well as a pseudo-static RAM mentioned above, or as a further alternative, may be a flash memory (EEPROM) or any of various ROMs or a small, thin rewritable optical disk.

The digital signal may be character or image information, or a combination of an audio signal and a character or image information as well as an audio signal mentioned above. For reproducing such character or audio information, a display unit is required. A display unit, though not specifically limited, may include a thin and lightweight liquid crystal display unit.

Claims

1. A digital information system comprising a digital signal source (100) and a device (101) separate from the signal source and having a memory (701) for storing a specified digital signal from said signal source (100) when connected thereto and for reproducing the stored signal,

   characterised in that the separate device is a memory card (101) portable by the respective user and having a playback function for the stored signal.

2. The system of claim 1, wherein the digital signal is transmitted between the signal source (100) and the memory card (101) at a rate higher than the signal is processed by said playback function.

3. The system of claim 1 or 2, wherein said signal source includes a terminal device (100) for storing a digital signal received from a supply through a selected communication channel (R-In, L-In, B-ISDN) and having a storage medium (301) for storing the received signal and an output unit (104) for connection to said memory card (101) and transmission of the specified signal.

4. The system of claim 3, wherein the capacity of the storage medium (301) in said terminal device (100) is equal to or larger than that of the memory (701) in the memory card (101).

5. The system of claim 3 or 4, wherein the storage medium in said terminal device (100) includes a magnetic disc memory (301) having a comparatively large storage capacity as a backup memory, and a high-speed accessible semiconductor buffer memory (308) for holding a signal to be transmitted from the magnetic disk memory (301) to said memory card (101).

6. The system of claim 5, wherein the terminal device (100) has a microcomputer function for managing the magnetic disk memory (301) and the buffer memory (403), for receiving digital signals through the respective communication channel (R-In, L-In, B-ISDN), and for managing the storage area of the memory (701) in the memory card (101) when connected to the terminal device (100).

waltung des Magnetplattenspeichers (301) und des Pufferspeichers (403), zum Empfangen von Digitalsignalen über den jeweiligen Übertragungskanal (R-In, L-In, B-ISDN) und zur Verwaltung des Speicherbereichs des Speichers (701) in der Speicherkarte (101) bei Verbindung mit dem Anschlußgerät (100) aufweist.

7. System nach einem der Ansprüche 3 bis 6, wobei das Anschlußgerät (100) die Wiedergabe- und Ausgabefunktion für einen Teil eines bezeichneten Signals über eine vorgegebene Zeitspanne aufweist.

8. System nach einem der vorhergehenden Ansprüche mit einer Einrichtung zur Kompression oder Dekompression der Informationsmenge im Vergleich zu der ursprünglichen Informationsmenge des Digitalsignals sowie einer Einrichtung (1500) zur Rauschunterdrückung.

9. System nach Anspruch 8, wobei die Rauschunterdrückungs-Einrichtung (1500) eine Einrichtung (1507, 1508) zum Erfassen eines Stimmintervalls eines digitalisierten Audiosignals sowie eine Einrichtung (1508, 151n) aufweist, die das einem Digital/Analog-Wandler zugeführte Digitalsignal durch ein einem Wechselstrom-Nullpegel entsprechendes Signal ersetzt.

10. System nach Anspruch 8 oder 9, wobei die Rauschunterdrückungs-Einrichtung (1500) eine Vergleicherstufe (1501, 1509) umfaßt, die ein Digitalsignal mit vorgegebenen positiven und negativen Signalen, die als stimmlos im Sinne eines Stimmintervalls gelten, vergleicht, wobei eine vorgegebene Periode mit vorgegebenem Pegel aufgrund des Vergleichsergebnisses als stimmlos bestimmt wird.

11. System nach Anspruch 8, wobei die Dekompressionseinrichtung ein Stimmintervall (3303, 3304) eines digitalisierten Audiosignals erfaßt und das Stimmintervall durch langsame Wiedergabe verlängert.

12. System nach Anspruch 11, wobei das besagte Stimmintervall dadurch verlängert wird, daß der Adressen-Auffrischvorgang des das Digitalsignal aufnehmenden Speichers gegenüber der normalen Arbeitsweise verzögert wird.

13. System nach Anspruch 8, wobei die Kompressionseinrichtung ein Stimmsignal (3303, 3304) eines digitalisierten Audiosignals erfaßt und das Stimmintervall durch schnelle Wiedergabe verkürzt.

14. System nach Anspruch 13, wobei das Stimmintervall dadurch verkürzt wird, daß die Geschwindigkeit des Adressen-Auffrischvorgangs des das Digitalsignal aufnehmenden Speichers gegenüber der normalen Arbeitsweise erhöht wird.

15. System nach Anspruch 8, wobei die Kompressionseinrichtung umfaßt:

eine Einrichtung (4402) zum Ermitteln der Differenz zwischen den unmittelbar vorhergehenden Abtastdaten des Digitalsignals und Eingangsdaten,

eine Einrichtung (4404), die den Maximalwert der komprimierten Daten ausgibt, wenn die Differenz den Maximalwert eines komprimierten Codes überschreitet, und

eine Einrichtung (4404), die das Ergebnis einer Subtraktion aufgrund der komprimierten Daten ausgibt, wenn die Differenz unter dem Maximalwert des komprimierten Codes liegt.

16. System nach Anspruch 8, wobei die Dekompressionseinrichtung die Daten des Digitalsignals durch Hinzufügen der unmittelbar vorhergehenden Abtastdaten auf die ursprünglichen Daten verlängert.

Revendications

1. Système d'information numérique comprenant une source de signaux numériques (100) et un dispositif (101) séparé de la source de signaux et possédant une mémoire (701) pour mémoriser un signal numérique spécifié provenant de ladite source de signaux (100), lorsque la mémoire est raccordée à cette source, et pour reproduire le signal mémorisé,

caractérisé en ce que le dispositif séparé est une carte de mémoire (101) portable par l'utilisateur respectif et possédant une fonction de lecture pour le signal mémorisé.

2. Système selon la revendication 1, dans lequel le signal numérique est transmis entre la source de signaux (100) et la carte de mémoire (101) à une vitesse supérieure à la vitesse de traitement du signal par ladite fonction de lecture.

3. Système selon la revendication 1 ou 2, dans lequel ladite source de signaux comprend un dispositif terminal (100) pour mémoriser un signal numérique reçu d'une source par l'intermédiaire d'un canal de communication sélectionné (R-In, L-In, B-ISDN) et possédant un milieu de mémoire (301) pour mémoriser le signal reçu et une unité de sortie (104) destinée à être raccordée à ladite carte de mémoire (101) et à transmettre le signal

FIG. 1

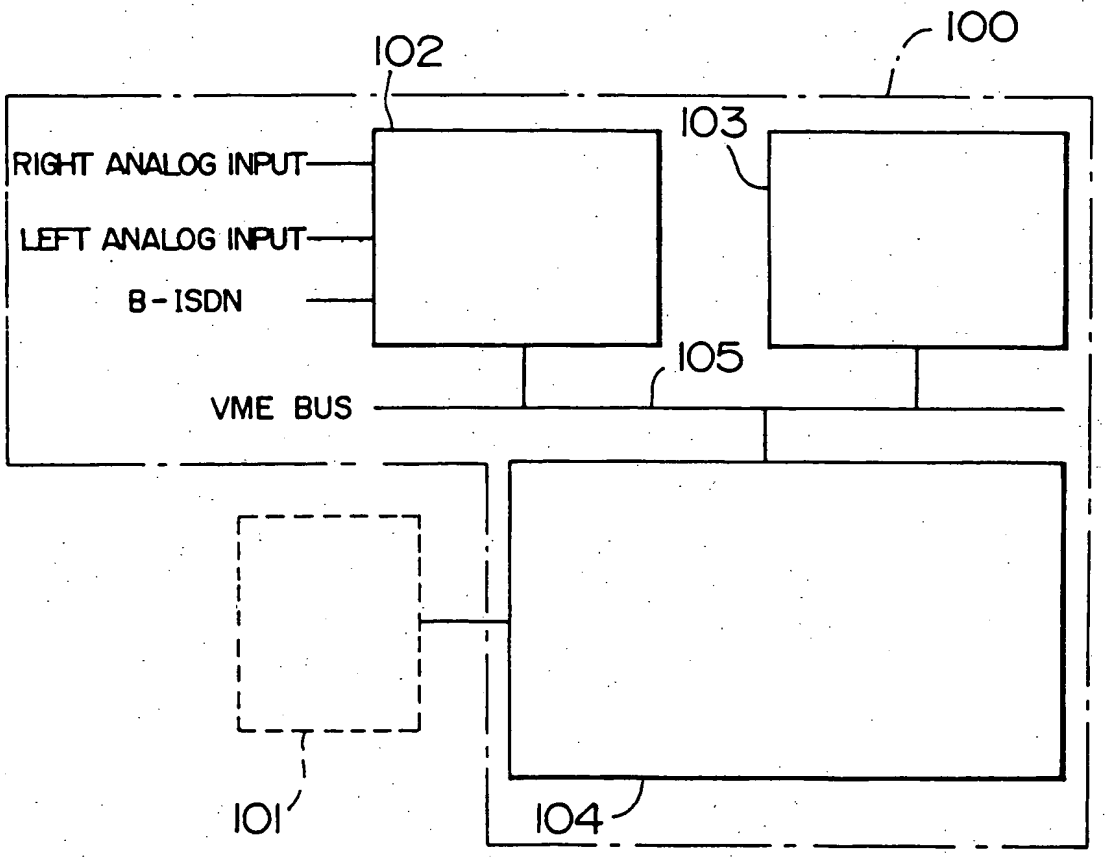
100
102
103
RIGHT ANALOG INPUT
LEFT ANALOG INPUT
B-ISDN
105
VME BUS
101
104

FIG. 4

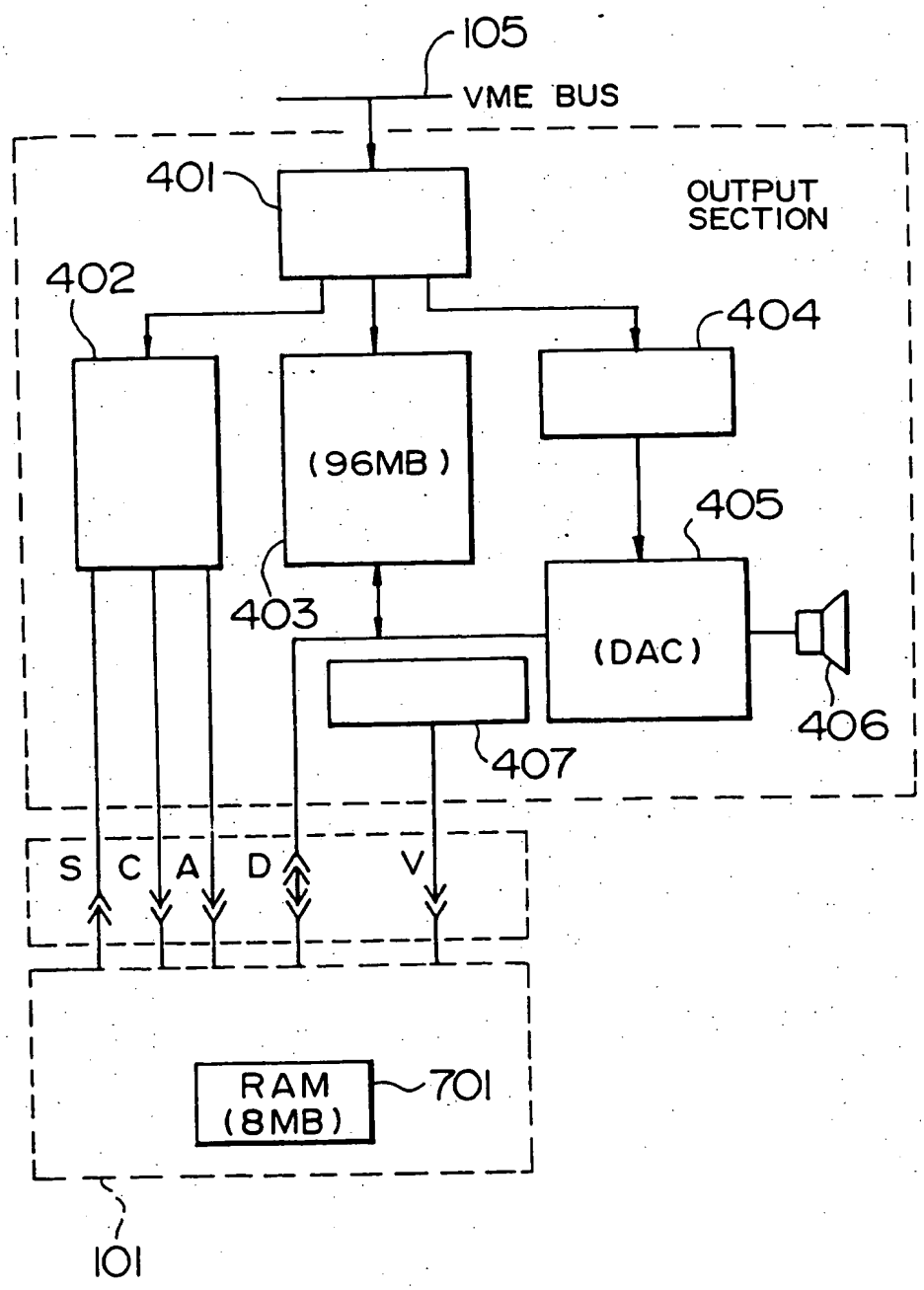
105
VME BUS
401
OUTPUT SECTION
402
404
(96MB)
405
403
(DAC)
406
407
S
C
A
D
V
RAM (8MB)
701
101

FIG. 6

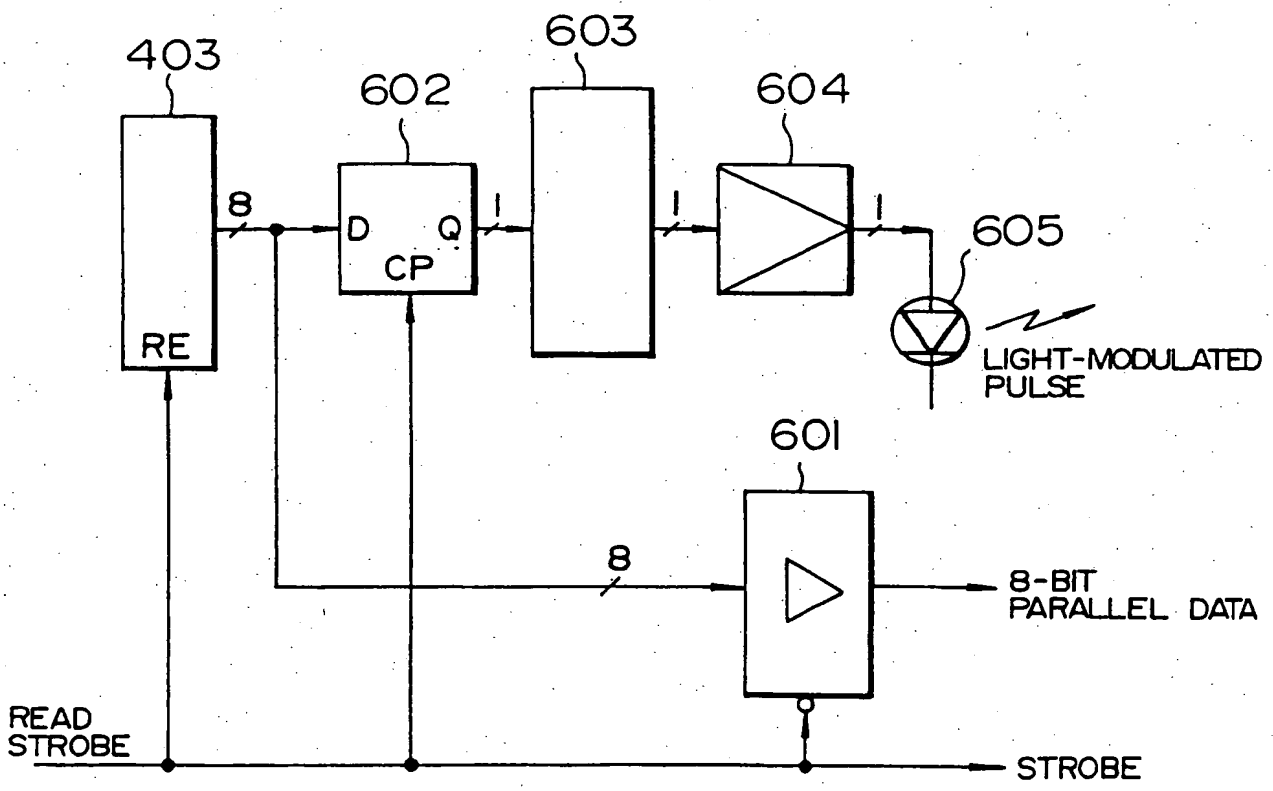
403
602
603
604
605
601
RE
8
D
Q
CP
1
1
1
8
8-BIT
PARALLEL DATA
LIGHT-MODULATED
PULSE
READ
STROBE
STROBE

FIG. 8

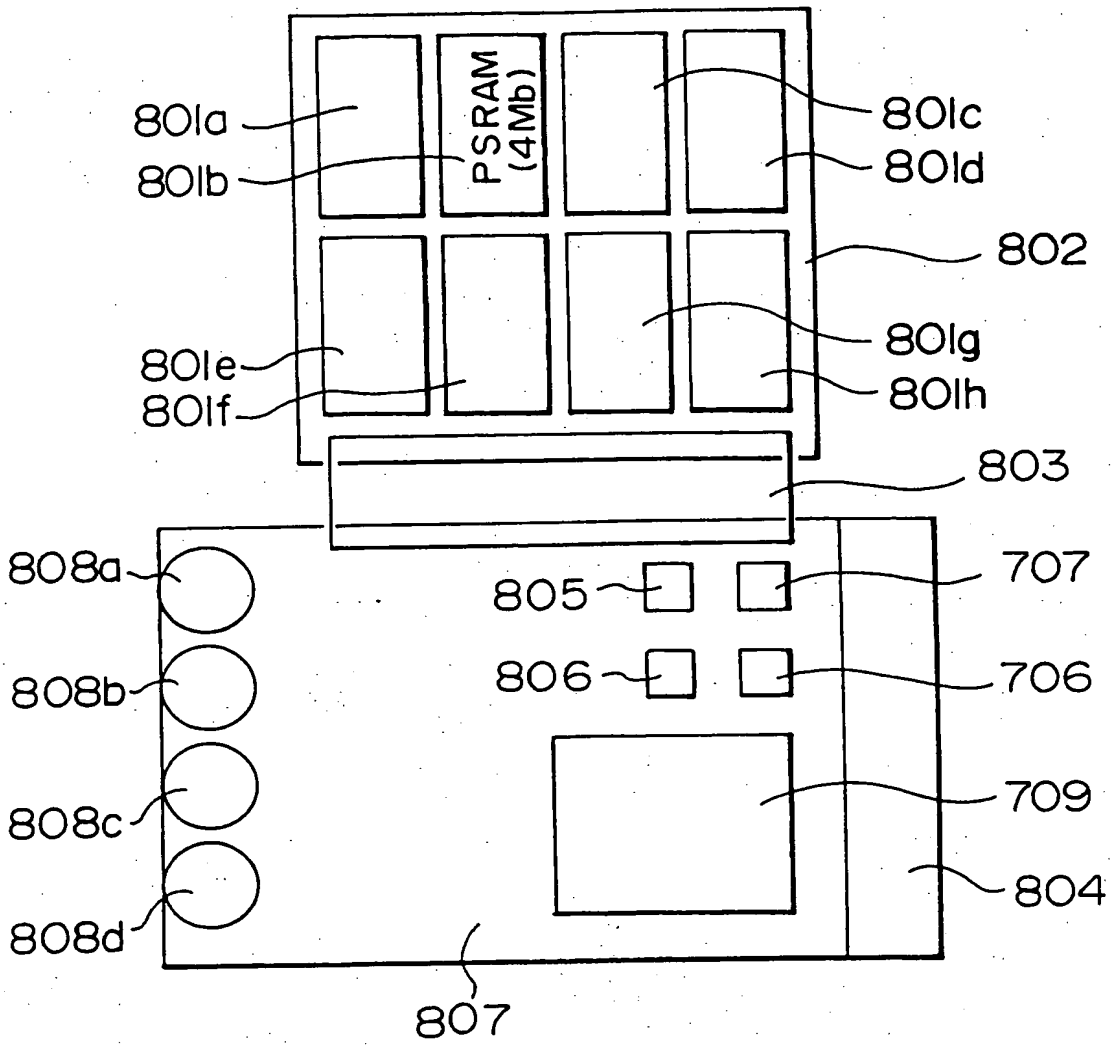
801a
801b
PSRAM (4Mb)
801c
801d
802
801e
801f
801g
801h
803
808a
808b
808c
808d
805
806
707
706
709
804
807

FIG. 9

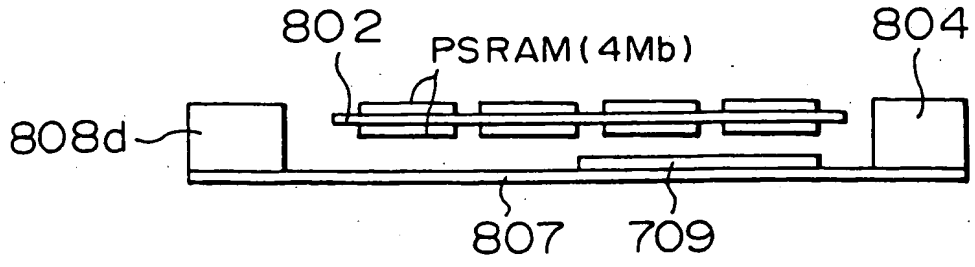
802
PSRAM(4Mb)
804
808d
807
709

FIG.12

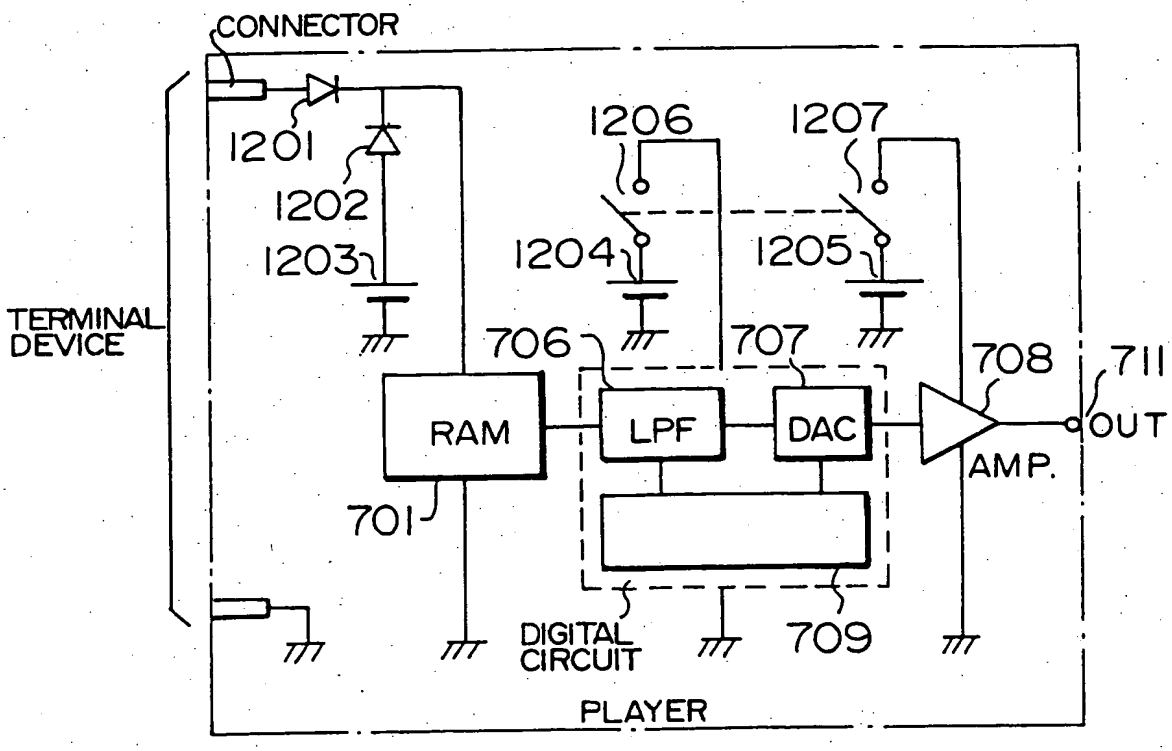
CONNECTOR
1201
1202
1203
1206
1207
1204
1205
TERMINAL DEVICE
706
707
708
711
RAM
LPF
DAC
AMP.
OUT
701
DIGITAL CIRCUIT
709
PLAYER

FIG.15

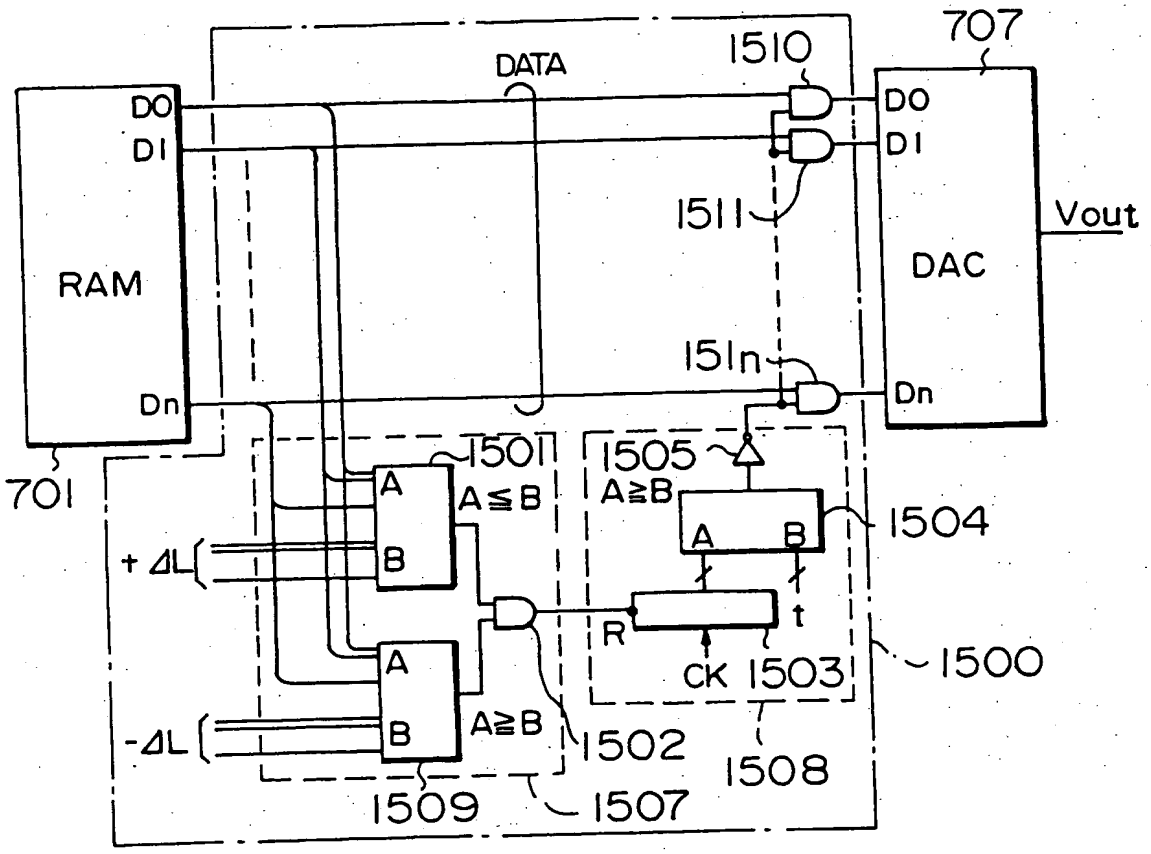
707
1510
DATA
DO
D1
RAM
Dn
701
1511
DAC
Vout
151n
1501
1505
A≧B
A≦B
A
B
+ΔL
-ΔL
1504
t
R
CK
1503
1500
1502
1508
1509
1507

FIG.16

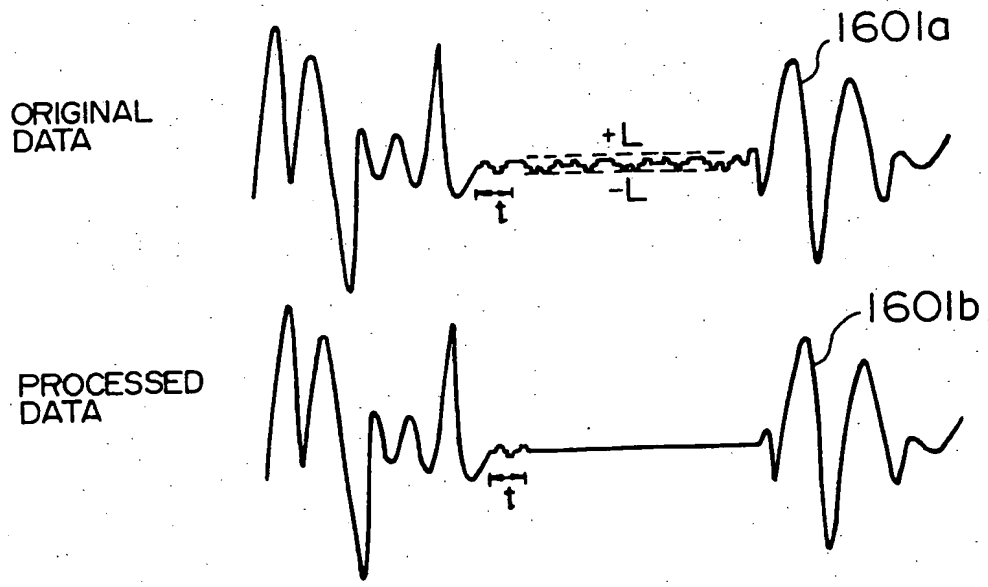
1601a
ORIGINAL DATA
+L
-L
t
1601b
PROCESSED DATA
t

FIG.19

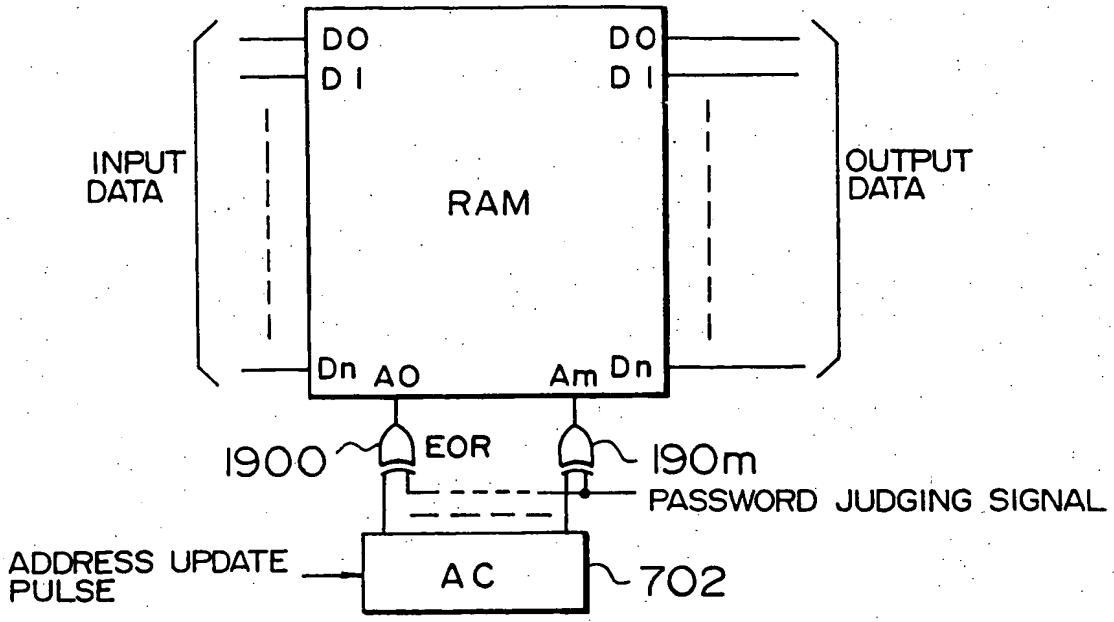
DO
DI
DO
DI
INPUT DATA
RAM
OUTPUT DATA
Dn AO
Am Dn
1900
EOR
190m
PASSWORD JUDGING SIGNAL
ADDRESS UPDATE PULSE
AC
702

FIG. 20

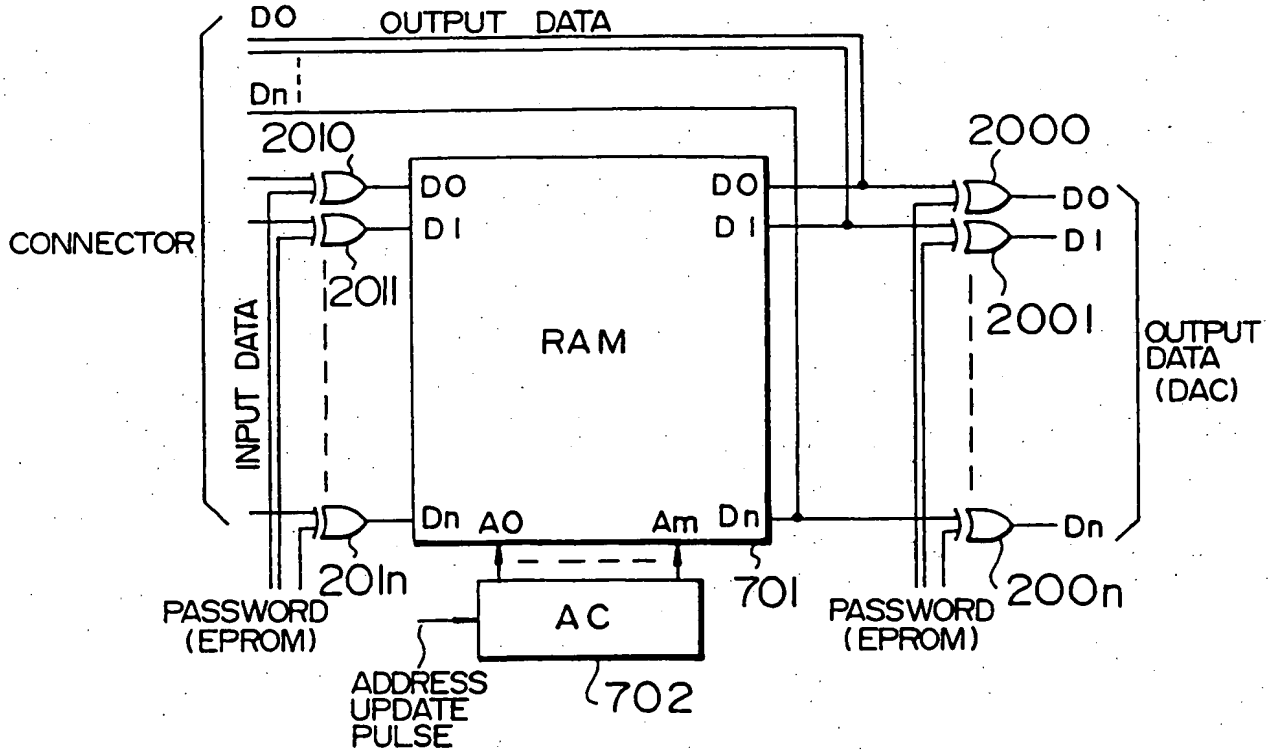
DO
OUTPUT DATA
Dn
2010
2000
CONNECTOR
DO
DI
DO
DI
2011
2001
INPUT DATA
RAM
OUTPUT DATA (DAC)
Dn AO
Am Dn
Dn
201n
701
200n
PASSWORD (EPROM)
AC
PASSWORD (EPROM)
ADDRESS UPDATE PULSE
702

FIG. 23

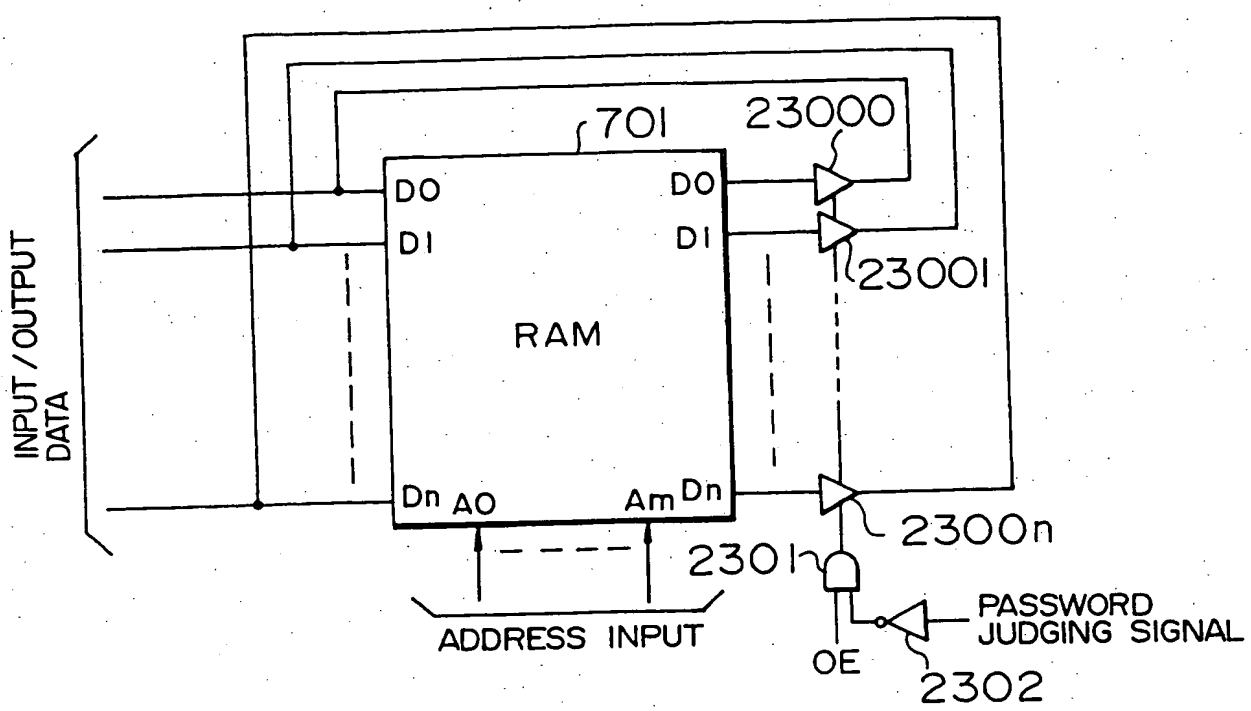
701
23000
DO
DI
DO
DI
23001
RAM
INPUT/OUTPUT DATA
Dn A0
Am Dn
2300n
2301
ADDRESS INPUT
PASSWORD JUDGING SIGNAL
OE
2302

FIG. 24

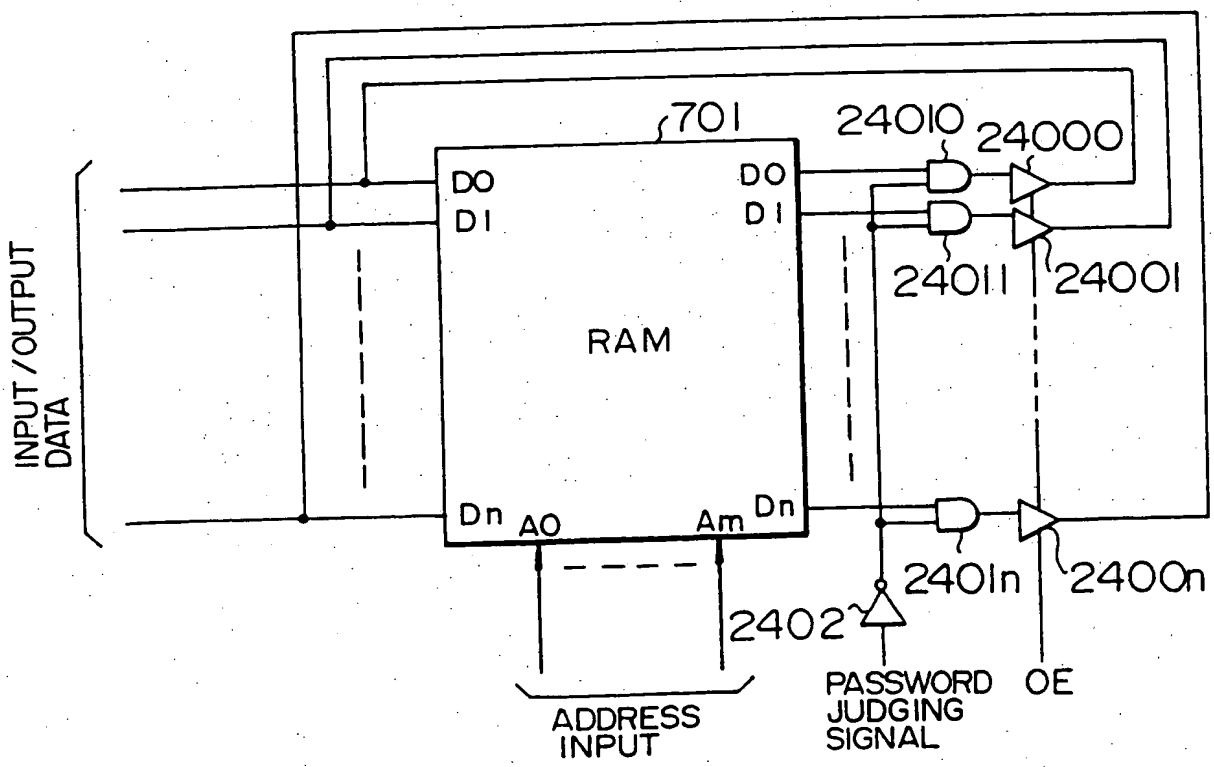
701
24010
24000
DO
DI
DO
DI
24011
24001
RAM
INPUT/OUTPUT DATA
Dn A0
Am Dn
2401n
2400n
2402
ADDRESS INPUT
PASSWORD JUDGING SIGNAL
OE

FIG.26

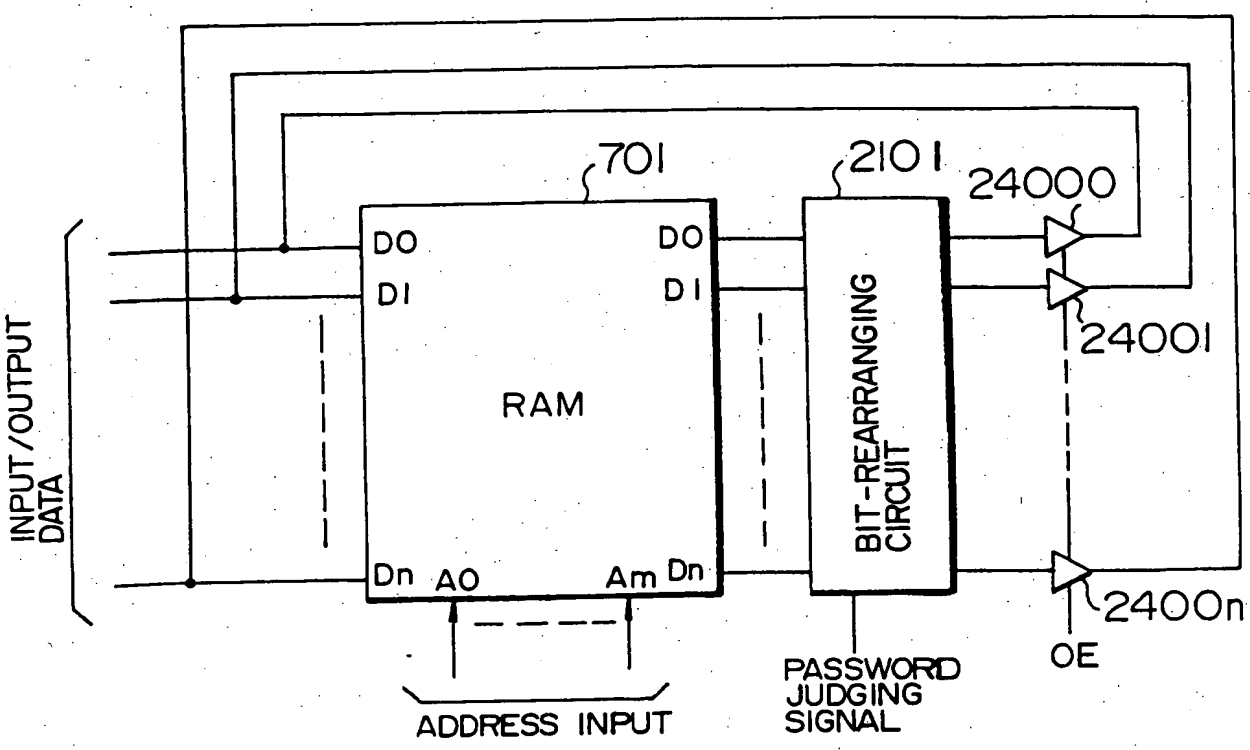
701
2101
24000
24001
2400n
DO
DI
RAM
Dn
A0
Am
BIT-REARRANGING CIRCUIT
INPUT/OUTPUT DATA
ADDRESS INPUT
PASSWORD JUDGING SIGNAL
OE

FIG.27

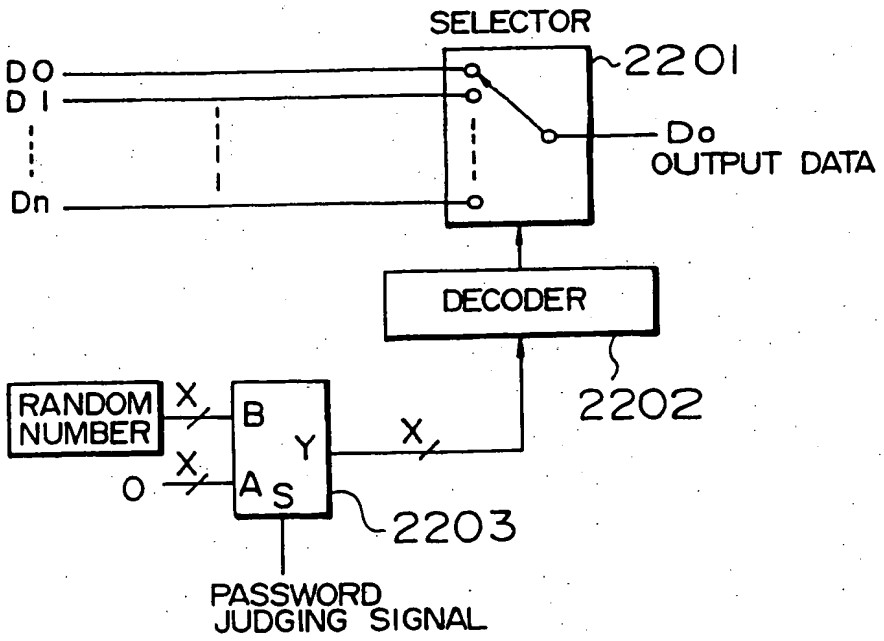
SELECTOR
2201
DO
DI
Dn
Do
OUTPUT DATA
DECODER
2202
RANDOM NUMBER
X
B
Y
X
0
X
A
S
2203
PASSWORD JUDGING SIGNAL

FIG. 30

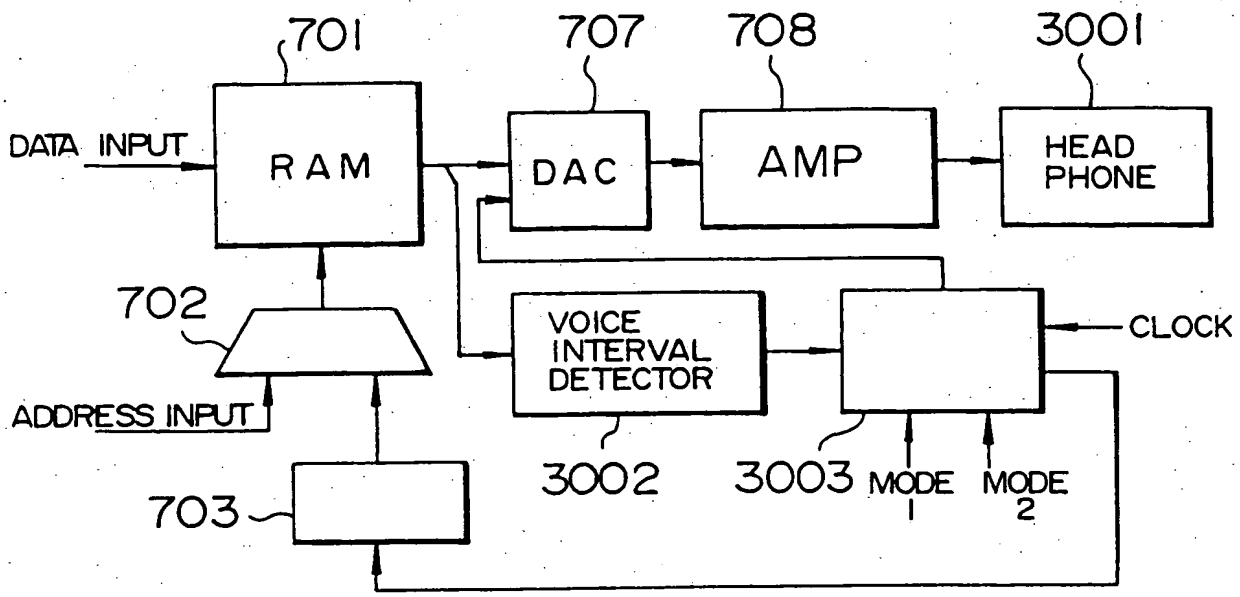
701
707
708
3001
DATA INPUT
RAM
DAC
AMP
HEAD PHONE
702
VOICE INTERVAL DETECTOR
CLOCK
ADDRESS INPUT
3002
3003
MODE 1
MODE 2
703

FIG. 31

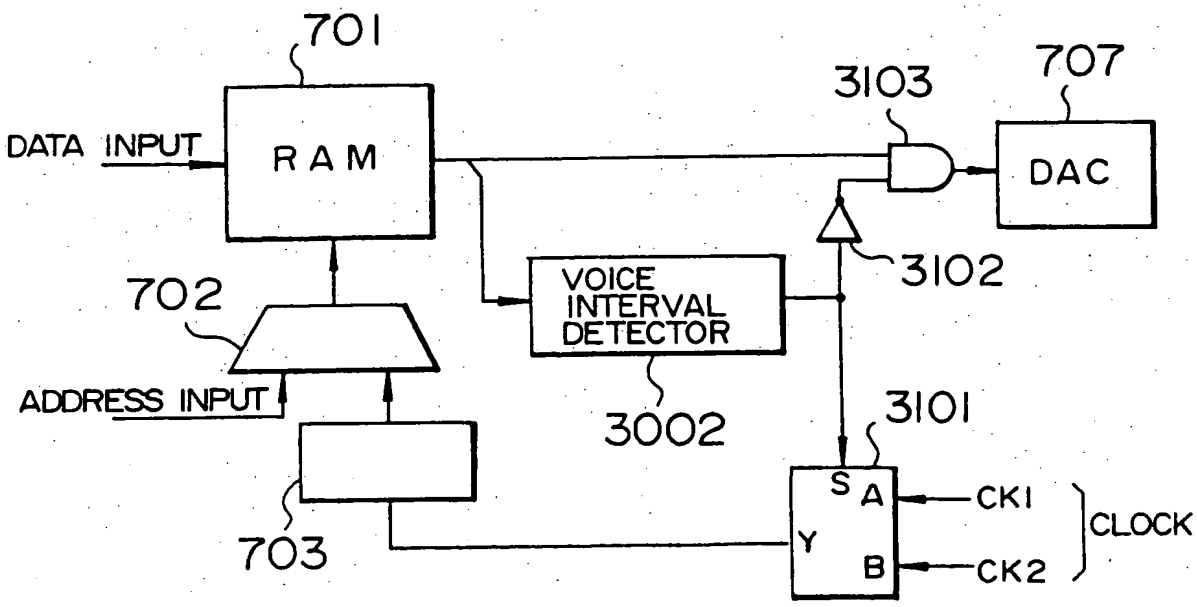
701
3103
707
DATA INPUT
RAM
DAC
3102
702
VOICE INTERVAL DETECTOR
ADDRESS INPUT
3002
3101
S
A
CK1
CLOCK
Y
B
CK2
703

FIG. 33

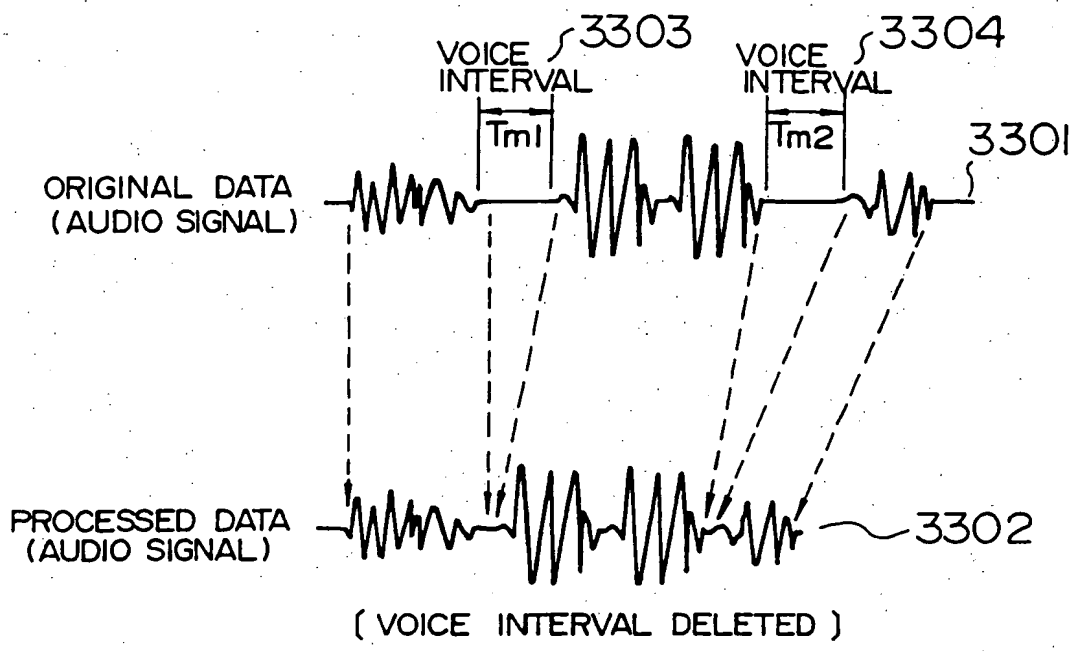
VOICE INTERVAL
3303
VOICE INTERVAL
3304
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
3302
(VOICE INTERVAL DELETED)

FIG. 34

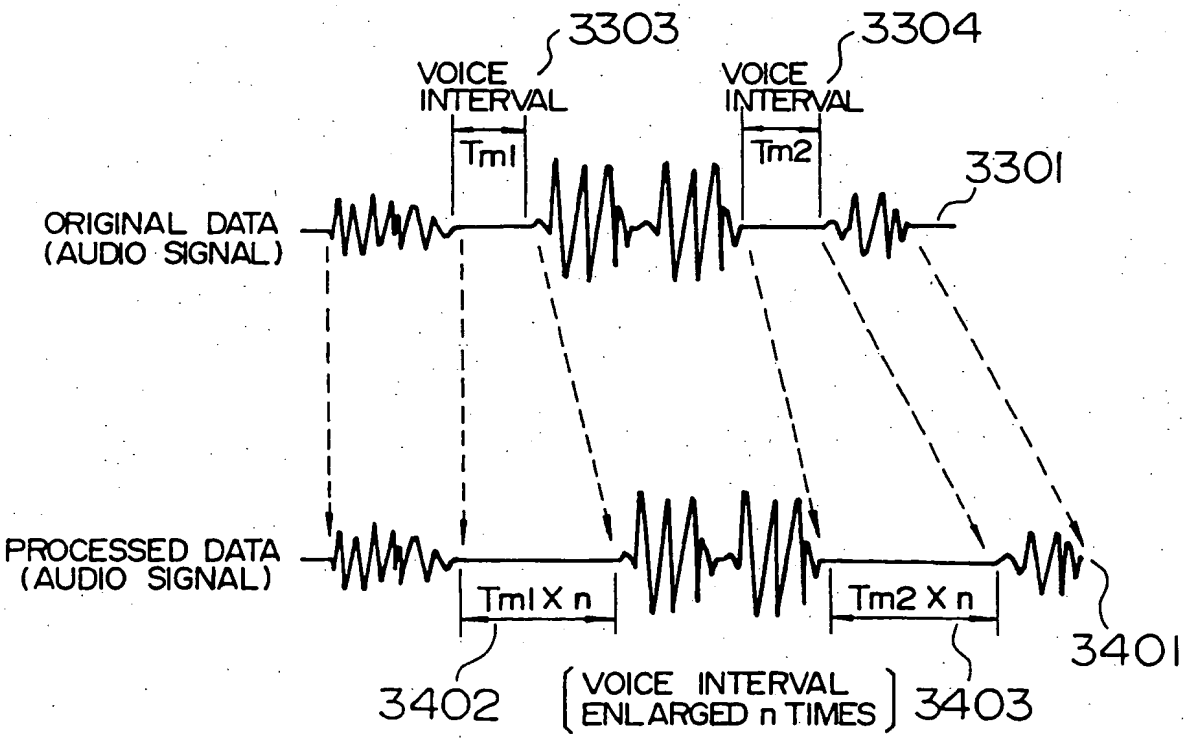
3303
VOICE INTERVAL
3304
VOICE INTERVAL
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
Tm1 X n
Tm2 X n
3401
3402
[VOICE INTERVAL ENLARGED n TIMES]
3403

FIG.37

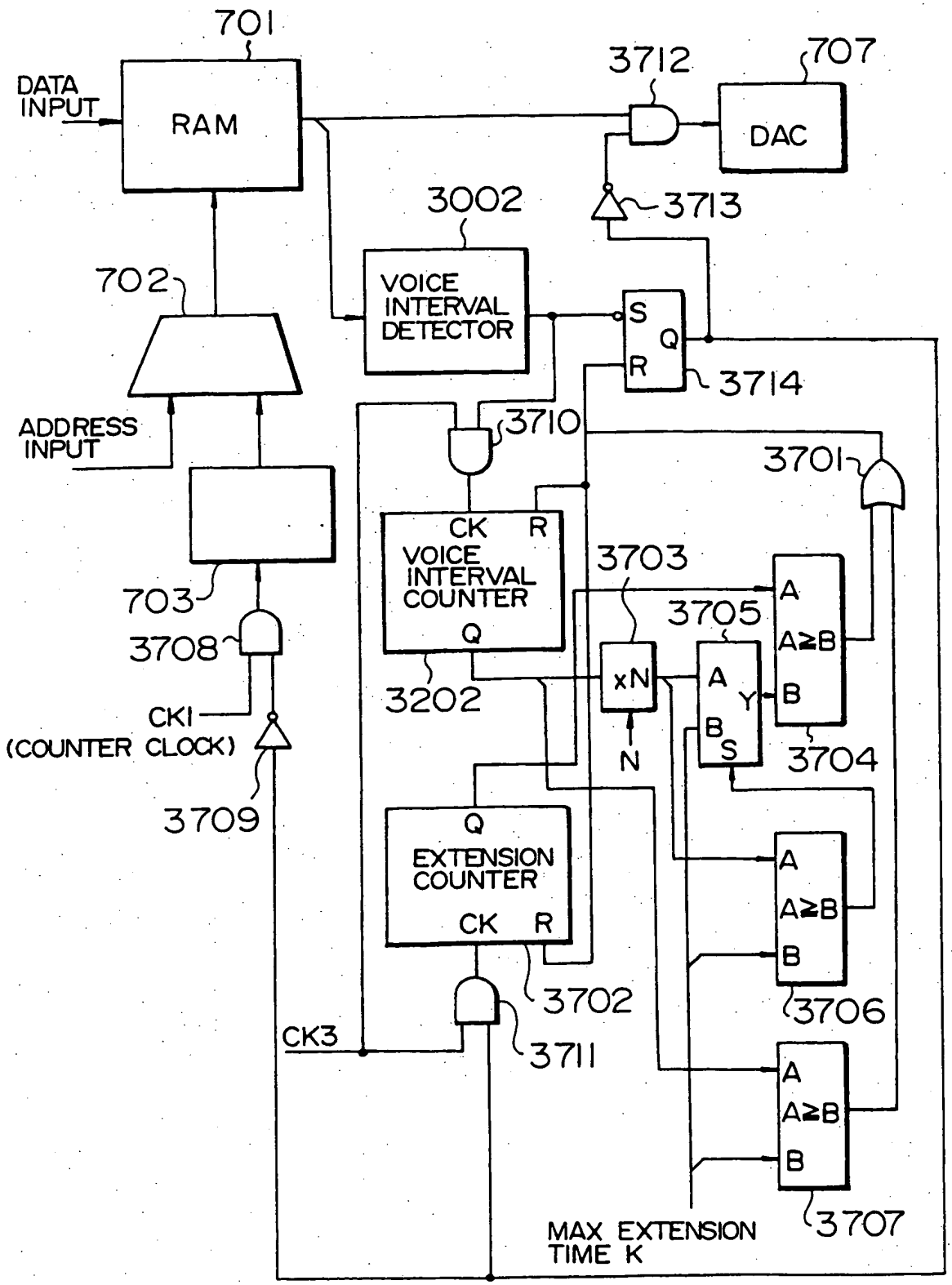
701
DATA INPUT
RAM
3712
707
DAC
3713
3002
VOICE INTERVAL DETECTOR
S
Q
R
3714
702
ADDRESS INPUT
3710
3701
CK R
VOICE INTERVAL COUNTER
Q
3202
703
3708
3703
3705
A
A≥B
B
xN
N
A
Y
B
S
3704
CKI
(COUNTER CLOCK)
3709
Q
EXTENSION COUNTER
CK R
3702
3706
CK3
3711
3707
MAX EXTENSION TIME K

FIG. 41

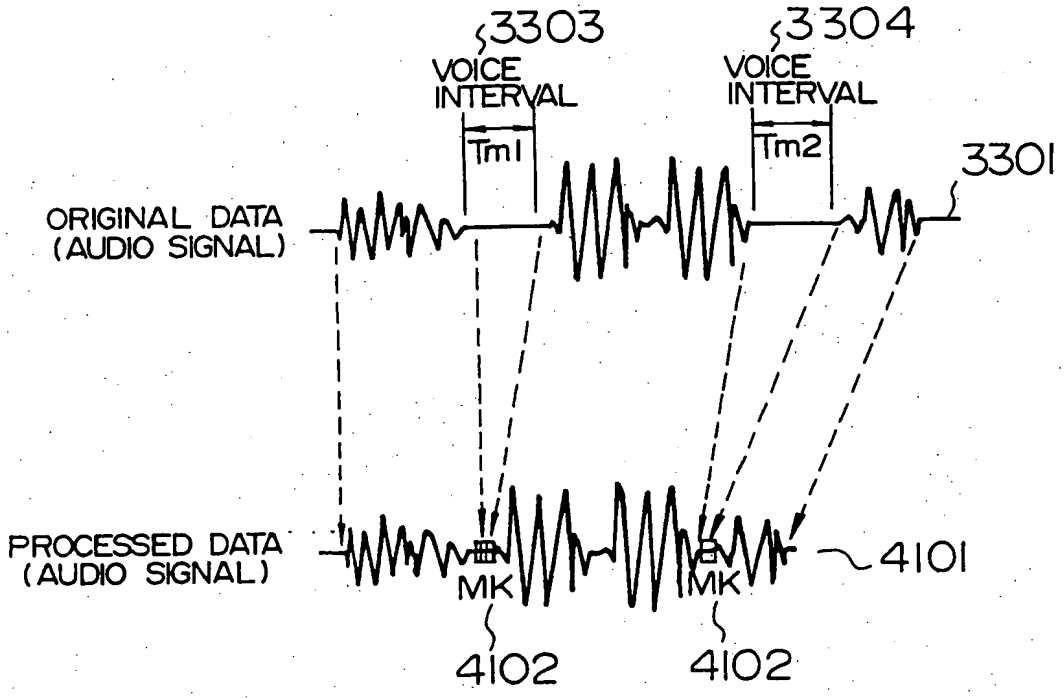
3303
3304
VOICE INTERVAL
VOICE INTERVAL
Tm1
Tm2
3301
ORIGINAL DATA (AUDIO SIGNAL)
PROCESSED DATA (AUDIO SIGNAL)
MK
MK
4101
4102
4102

FIG. 42

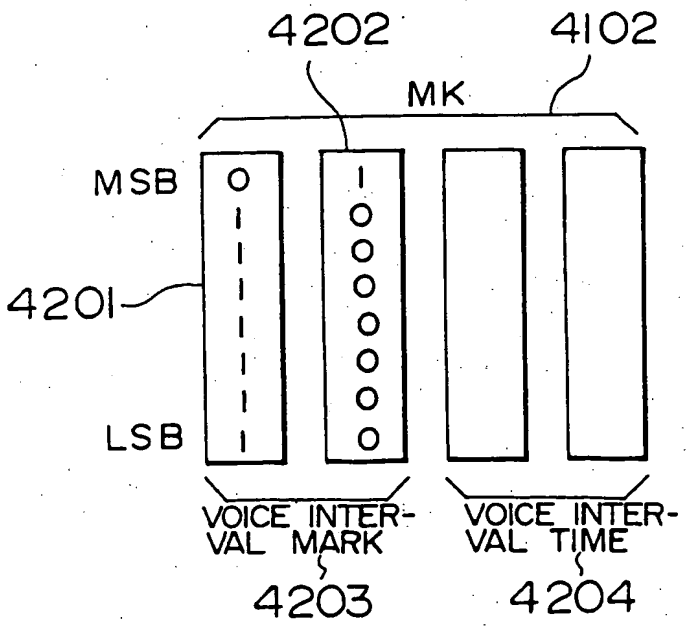
4202
4102
MK
MSB
4201
LSB
VOICE INTERVAL MARK
VOICE INTERVAL TIME
4203
4204

FIG. 44

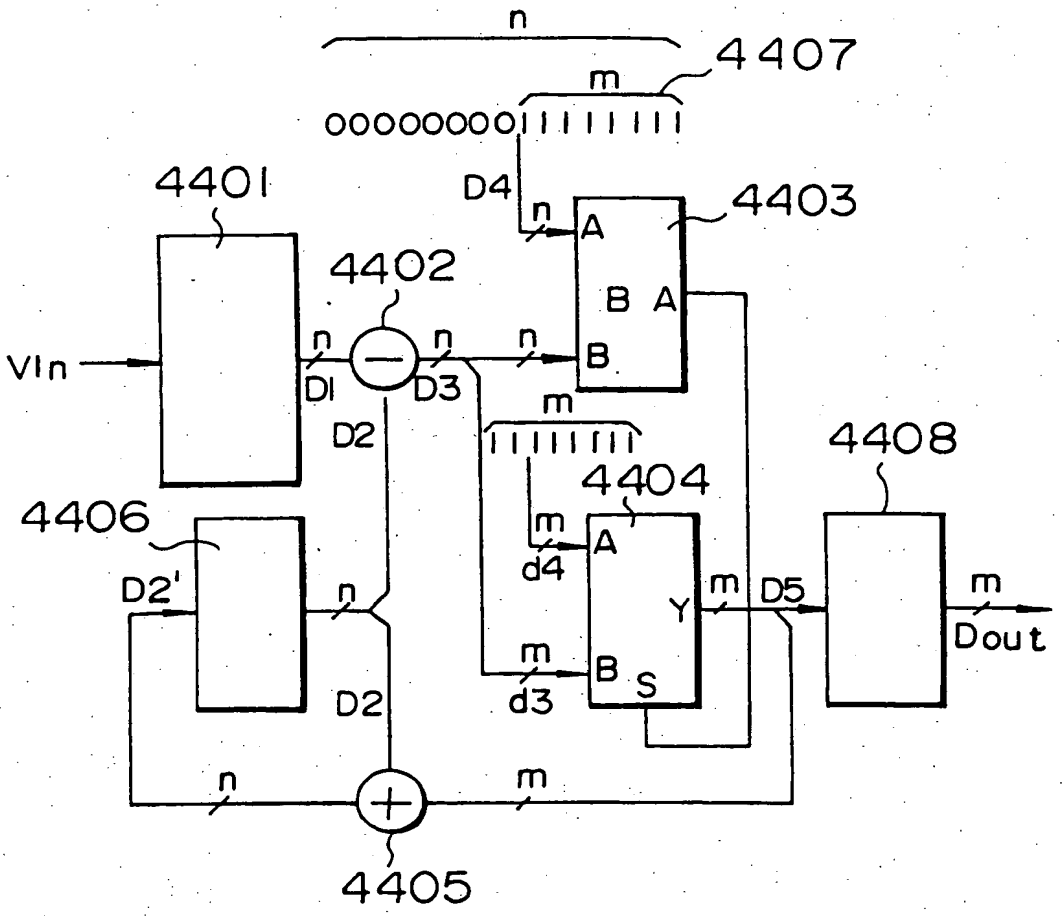
n
4407
m
00000000 11111111
4401
D4
n
A
4403
4402
B A
VIn
n
n
n
B
D1
D3
m
D2
4408
4404
4406
m
A
d4
D2'
n
m
D5
m
Y
Dout
m
B
S
d3
D2
n
m
4405

FIG. 47

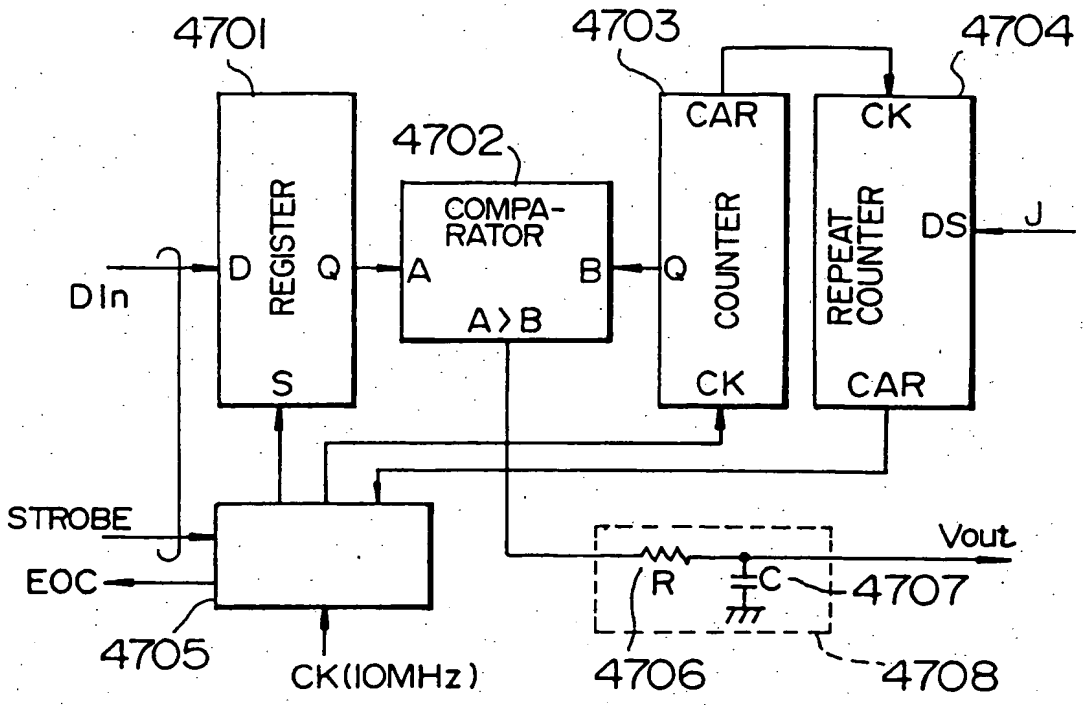
4701
4703
4704
4702
REGISTER
COMPA-
RATOR
COUNTER
REPEAT
COUNTER
CAR
CK
DS
J
D
Q
A
B
A>B
S
DIn
STROBE
EOC
Vout
R
C
4707
4705
CK(10MHz)
4706
4708

FIG. 48

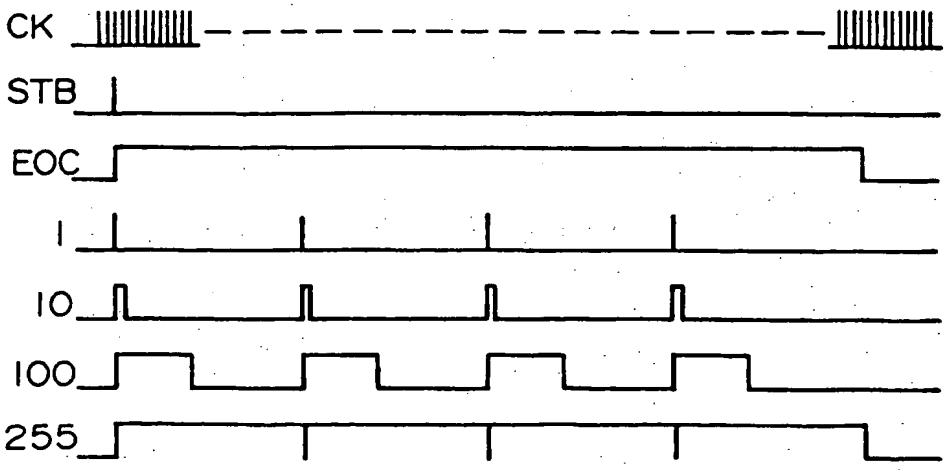
CK
STB
EOC
1
10
100
255

FIG. 50

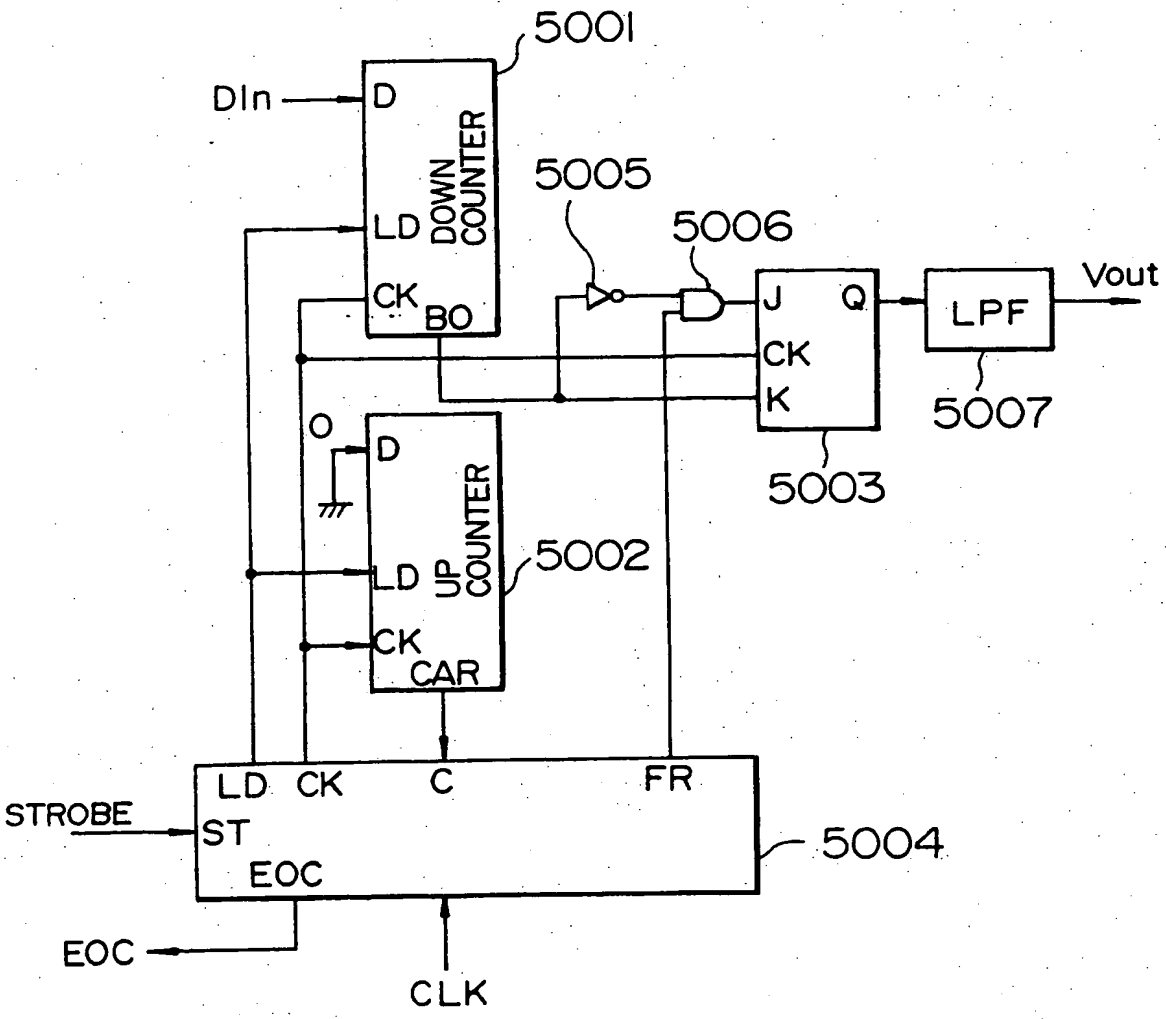
5001
DIn
D
LD
DOWN COUNTER
CK
BO
5005
5006
J
Q
CK
K
LPF
Vout
5007
5003
O
D
LD
UP COUNTER
5002
CK
CAR
LD
CK
C
FR
STROBE
ST
EOC
5004
EOC
CLK

FIG. 54

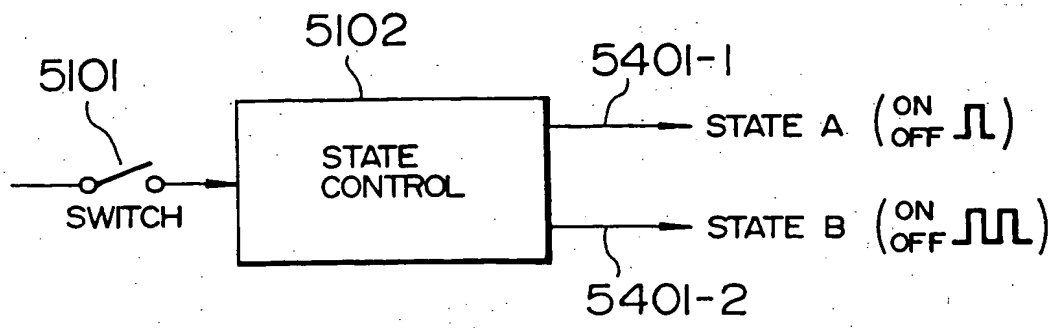
5102
5101
5401-1
STATE CONTROL
SWITCH
STATE A
ON
OFF
STATE B
ON
OFF
5401-2

FIG. 55

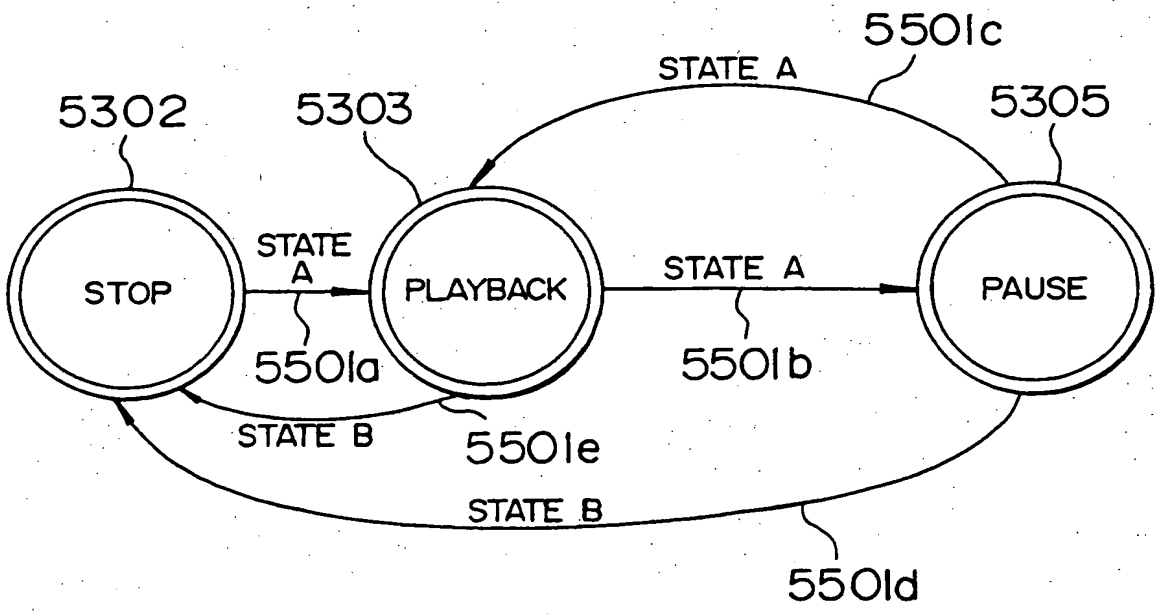
5501c
STATE A
5302
5303
5305
STOP
STATE A
PLAYBACK
STATE A
PAUSE
5501a
5501b
STATE B
5501e
STATE B
5501d

FIG. 57

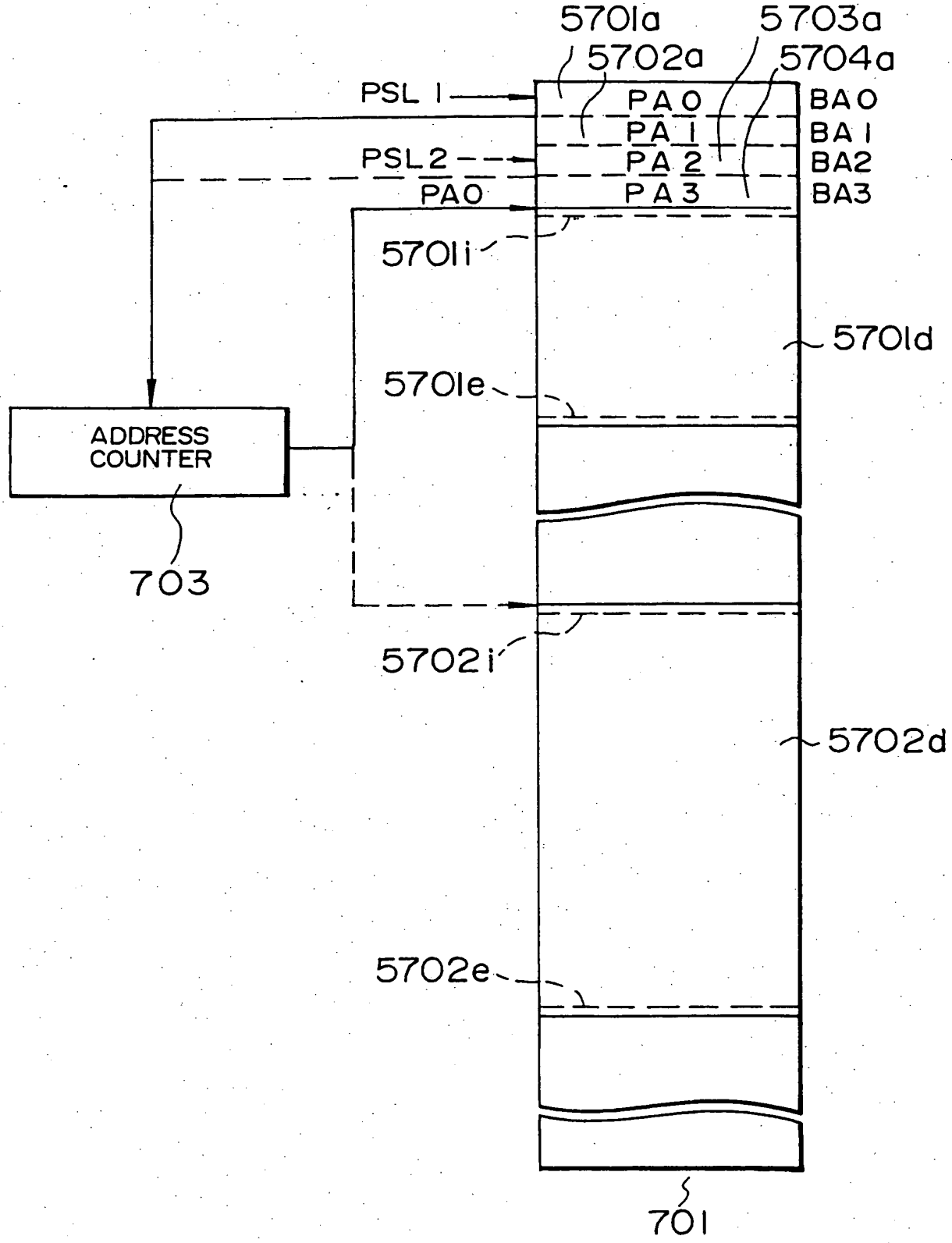
5701a
5703a
5702a
5704a
PSL 1
PSL2
PA0
PA 1
PA 2
PA 3
BA0
BA 1
BA2
BA3
5701i
5701d
5701e
ADDRESS COUNTER
703
5702i
5702d
5702e
701

FIG. 59

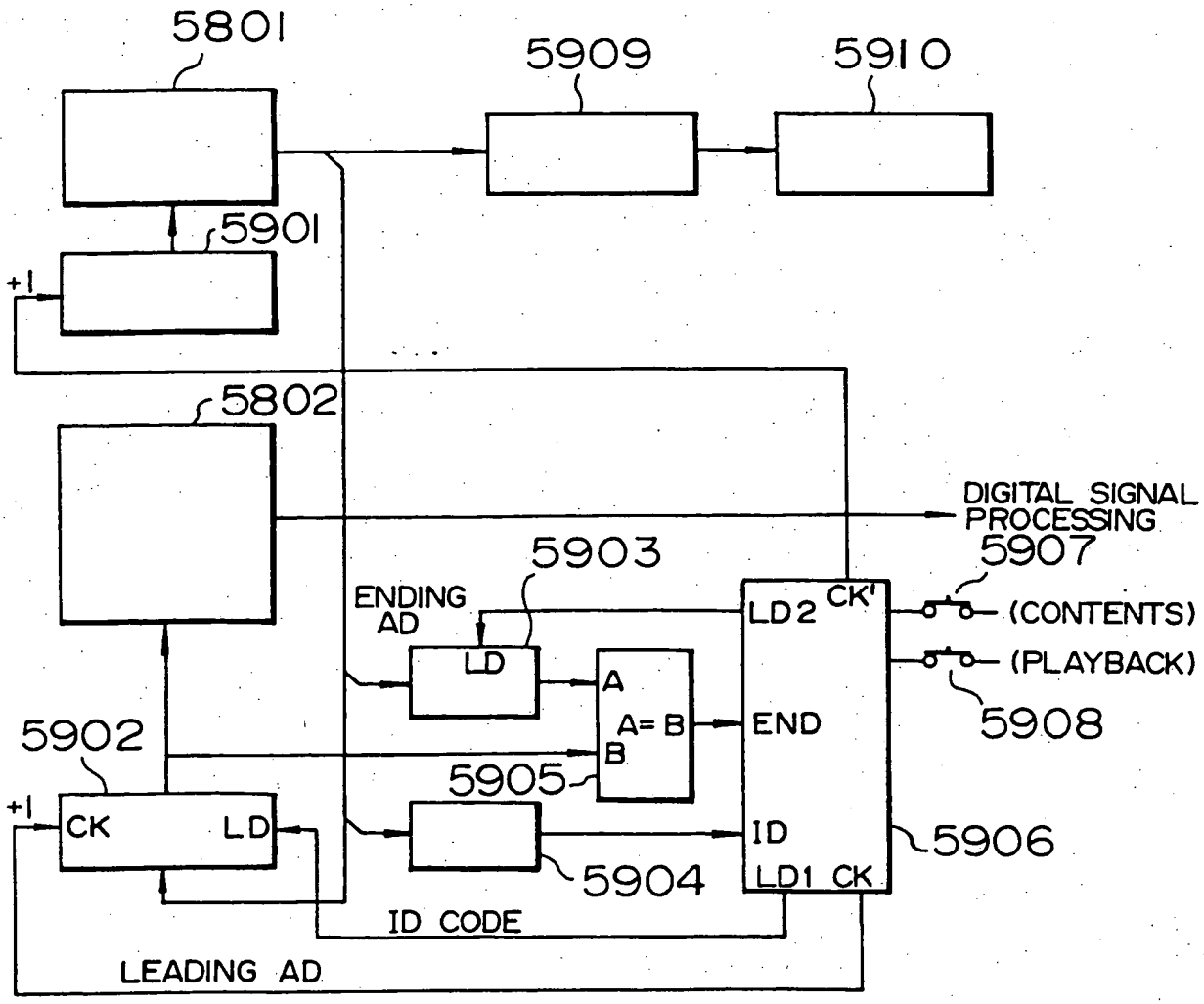
5801
5909
5910
5901
+1
5802
DIGITAL SIGNAL PROCESSING
5903
5907
ENDING AD
LD2
CK'
(CONTENTS)
LD
A
(PLAYBACK)
5908
5902
A= B
END
B
5905
+1
CK
LD
ID
5906
5904
LD1
CK
ID CODE
LEADING AD

FIG. 61

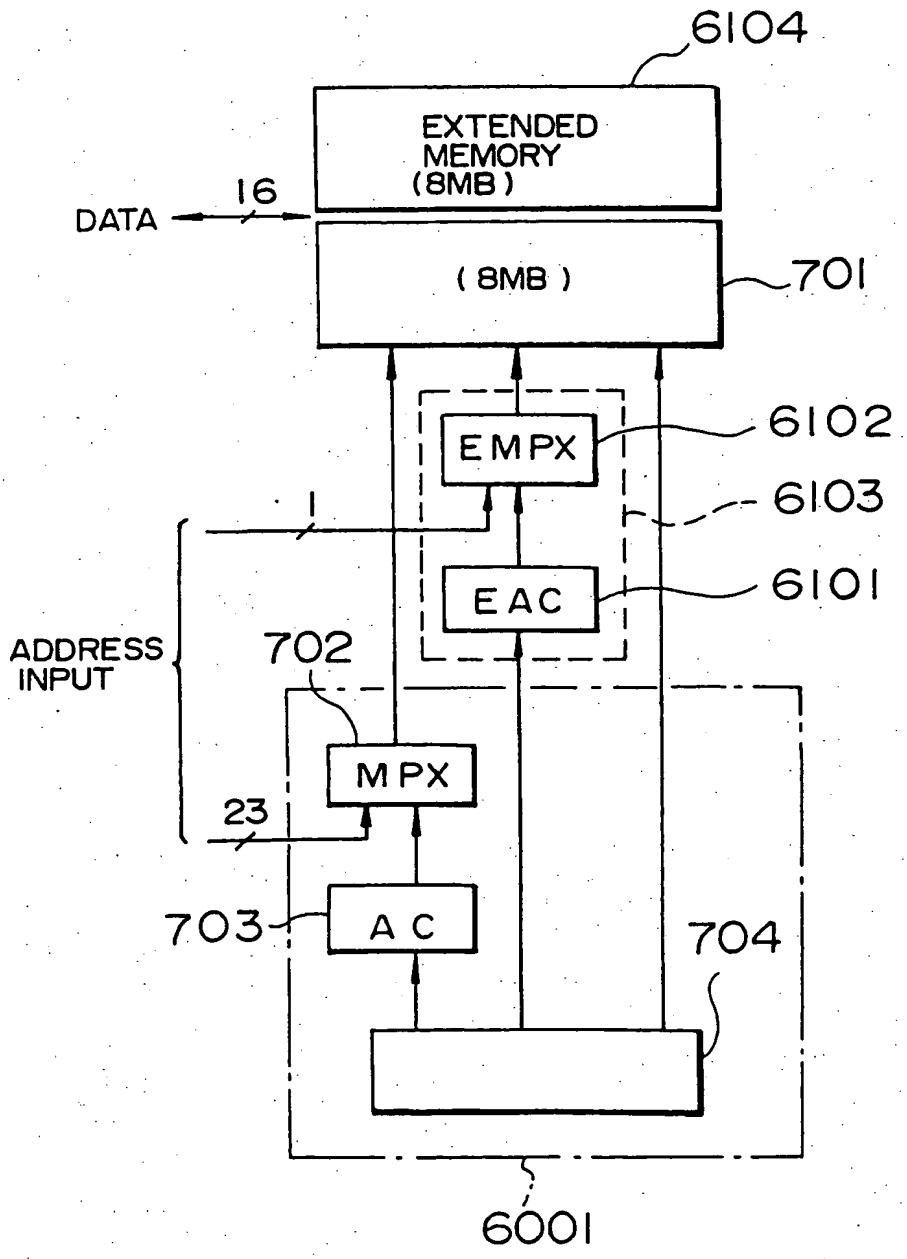
6104
EXTENDED MEMORY (8MB)
DATA
16
(8MB)
701
EMPX
6102
6103
1
EAC
6101
ADDRESS INPUT
702
MPX
23
703
AC
704
6001

FIG. 63

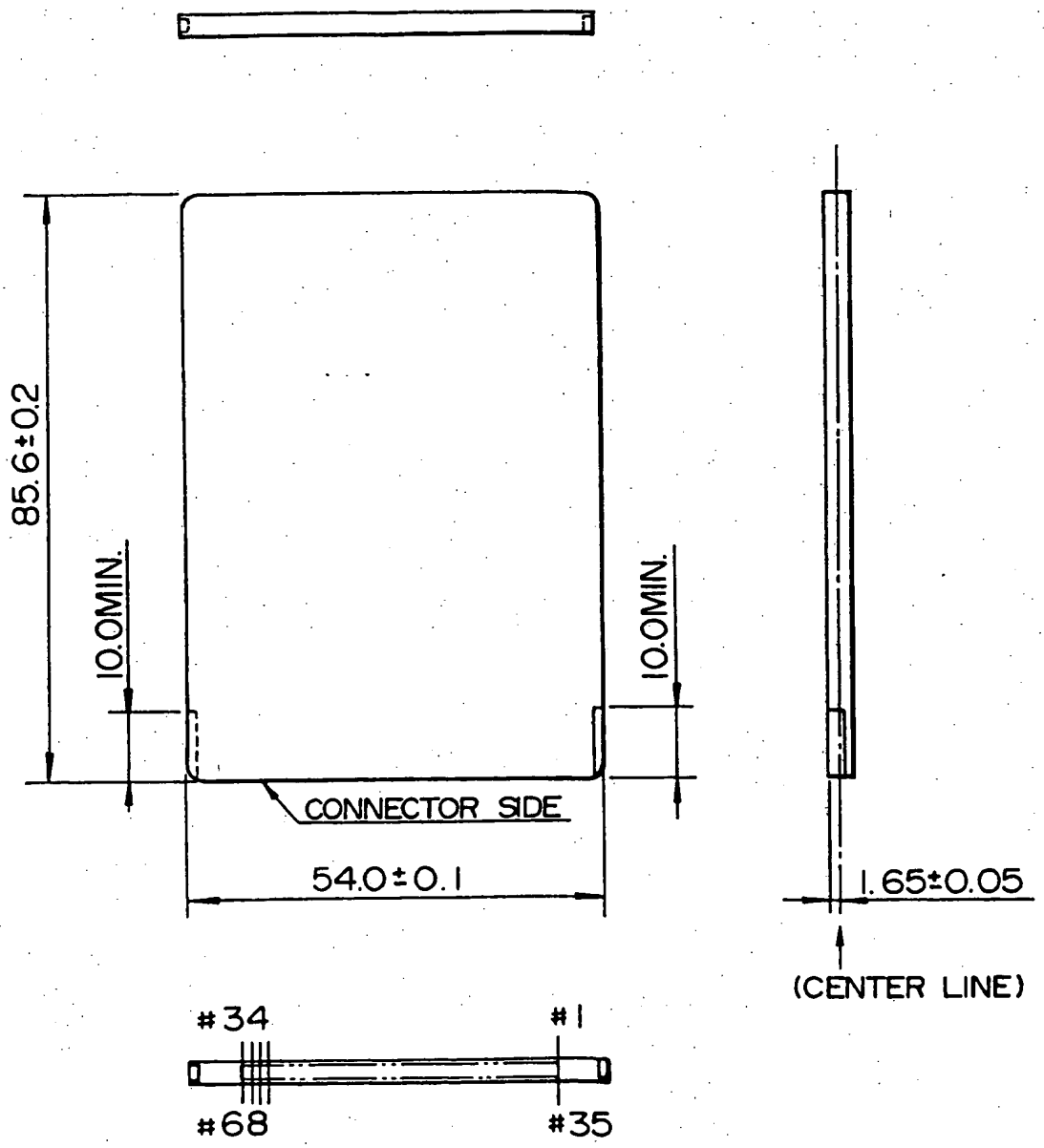
85.6±0.2
10.0MIN.
10.0MIN.
CONNECTOR SIDE
54.0±0.1
1.65±0.05
(CENTER LINE)
#34
#1
#68
#35

FIG.65

PIN	NAME	I/O	FUNCTION	PIN	NAME	I/O	FUNCTION
1	GND			35	GND		
2	D3	I/O		36	CD1	O	CARD DETECTION
3	D4	I/O		37	D11	I/O	
4	D5	I/O		38	D12	I/O	
5	D6	I/O		39	D13	I/O	
6	D7	I/O		40	D14	I/O	
7	$\overline{CE1}$	I	CARD ENABLE	41	D15	I/O	
8	A10	I		42	$\overline{CE2}$	I	CARD ENABLE
9	$\overline{OE}$	I	OUTPUT ENABLE	43	$\overline{RFSH}$	I	REFRESH (FOR PSRAM)
10	A11	I		44	RFU	NC	RESERVE
11	A9	I		45	RFU	NC	RESERVE
12	A8	I		46	A17	I	
13	A13	I		47	A18	I	
14	A14	I		48	A19	I	
15	$\overline{WE}/\overline{PGM}$	I	WRITE ENABLE	49	A20	I	
16	RDY/$\overline{BSY}$	O	RDY $\overline{BSY}$(EEPROM)	50	A21	I	
17	VCC			51	VCC		
18	VPP1		PROGRAM POWER (EVEN-NUMBERED BYTES)	52	VPP2		PROGRAM POWER (ODD-NUMBERED BYTES)
19	A16	I		53	A22	I	
20	A15	I		54	A23	I	
21	A12	I		55	A24	I	
22	A7	I		56	A25	I	
23	A6	I		57	RFU	NC	RESERVE
24	A5	I		58	RFU	NC	RESERVE
25	A4	I		59	RFU	NC	RESERVE
26	A3	I		60	RFU	NC	RESERVE
27	A2	I		61	$\overline{REG}$	I	ATTRIBUTE MEMORY SELECTION
28	A1	I		62	BVD2	O	BATTERY VOLTAGE DETECTION
29	A0	I		63	BVD1	O	
30	D0	I/O		64	D8	I/O	
31	D1	I/O		65	D9	I/O	
32	D2	I/O		66	D10	I/O	
33	WP	O	WRITE PROTECT	67	$\overline{CD2}$	O	CARD DETECTION
34	GND			68	GND		

FIG. 67